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DOCUMENT CHANGE SUMMARY

At Data I/O, we continually strive to improve our instruments as soon as they are developed. Sometimes, because of printing and shipping requirements, we can't include these changes immediately into printed manuals. Consequently, your manual may contain new change information as summarized below.

File the Documentation Change Summary and the Document Change Record pages in the beginning of your manual, in front of the Title Page. File any Document Addendum pages received with changes immediately after the other two Document Change pages. If you have received revised pages, remove the previous page version, and replace it with the latest page revision. If you have received a complete revision, remove all previously filed Document Addendums and replace the existing manual pages with the revised manual pages. Whenever you receive a manual update, replace the existing Document Change pages with the most recent set of Document Change pages.

REV	DESCRIPTION OF CHANGE	DATE
G	Incorporate ECN# 4998. Upgrade to program more devices.	12/83
H	Incorporate ECN #5025, resistor change to 30-702-1643, and transistor-mounting improvement to 30-701-1673.	2/84
J	ECP #0021, add 64k x 8 RAM configuration to model 120.	6/84
K	ECP #0025, software change.	7/84
L	ECP #0080, software change.	10/84

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DOCUMENT CHANGE REVISED PAGES RECORD

REVISED				ADDED		DELETED	
PAGE NUMBER	REV & DATE	PAGE NUMBER	REV & DATE	PAGE NUMBER	REV & DATE	PAGE NUMBER	REV & DATE
Title Page	L 10/84	Page 2-8	K 7/84				
Page 1-2	J 6/84	Page 3-1	K 7/84				
Page 1-3	K 7/84	Page 3-34	K 7/84				
Page 1-4	K 7/84	Page 4-3	K 7/84				
Page 2-5	K 7/84	Page 5-1	L 10/84				
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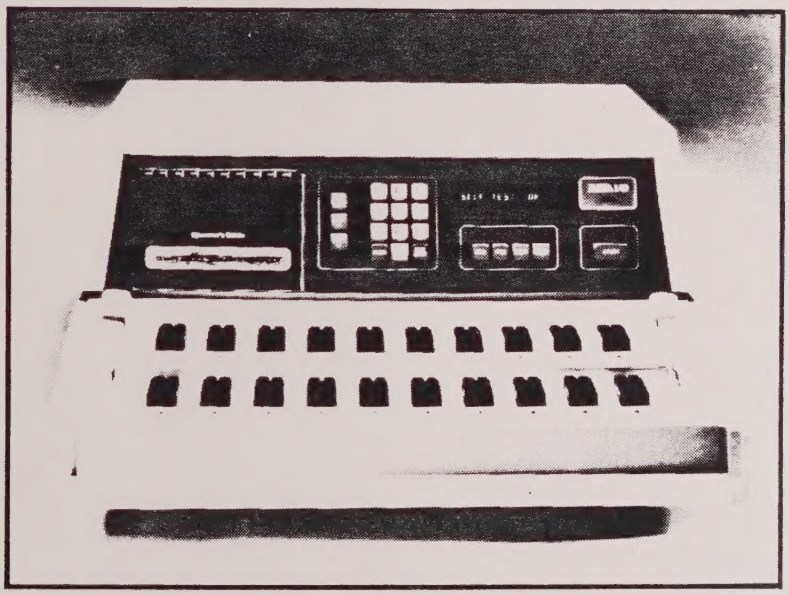

120A/121A
GANG PROGRAMMER

10-990-0120 REV L **NOVEMBER 84**

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Applies to: Engineering Part Numbers 990-0120-023 through -026
and 990-0121-061 through -068

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NOTE

This manual documents both the 120A and 121A programmers. Except where noted in bold print, the contents of this manual refer to both programmers.

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SECTION 1
INTRODUCTION

1.1 GENERAL INFORMATION

Data I/O's 120A and 121A Gang Programmers are rugged and dependable instruments that program MOS and CMOS PROMs, EPROMs and EEPROMs. The PROMs can be programmed as many as 20 at a time and do not require any special socket adapters or personality modules. You can select the type of device that you wish to program by entering the appropriate Family and Pinout codes at the front panel. Or if you are programming a large quantity of one type of device each time, you can set your programmer to default to that device. The programmer also supports an electronic identifier mode which reads the electronic identification from the inserted device(s) and automatically selects the appropriate family and pinout codes. Specific devices which the 120A and 121A program are listed in Table 1-4.

A special feature of the 121A is the ability to program sets of devices. In set programming the data in RAM is partitioned into blocks. Each block of data corresponds to a specific device in each set, and the device is programmed with that information. For example, you can simultaneously program two sets of eight 32K x 8 PROMs (27256) from a single 256K x 8 block of RAM data.

Your programmer can be operated from the front panel or through remote control, giving you greater flexibility in the workplace. Once the PROMs have been programmed, quick release bails provide an easy way to release the devices from their sockets.

Finally, your programmer can communicate with all compatible RS232C serial units. These include Data I/O's Data Control Unit (DCU), Paper Tape Reader/Punch and other data-transmitting and storage equipment.

1.2 SPECIFICATIONS

The following paragraphs describe the major components and power requirements of your programmer. Table 1-1 gives the physical and environmental specifications, and Table 1-2 lists the data translation formats available.

1.2.1 MAJOR COMPONENTS

The unit is microprocessor-controlled (6809E) and has a 32K x 8, 64K x 8, 128K x 8 or 256K x 8 data RAM, depending on the configuration. The 121A has two RS232C serial ports -either of which can be used to accept or transmit data.

All programming electronics are contained within the base unit. Therefore, there is no need for extra programming modules. Voltages are current-limited and regulated to meet the device manufacturers' programming specifications.

1.2.2 POWER REQUIREMENTS

The following are the 120A/121A's power requirements. Section 2.3 discusses power connection.

Operating Voltages. 100, 120, 220 or 240 V, +5%/-10%.

Frequency Range. 48-62Hz.

Power Consumption. 165W nominal.

A line fuse is located at the rear of the unit next to the AC power connector. The power supply is separately fuse.

1.2.3 PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

Table 1-1 lists the physical and environmental specifications of the 120A/121A.

Table 1-1. Physical and Environmental Specifications

Dimensions	56cm x 27cm x 66 cm (21 1/2" x 9 5/8" x 24")
Weight	21 kg (46 lb. 10 oz.)
Operating Temperature Range	5° to 45° C (41° to 113° F)
Storage Temperature Range	−40° to 70°C (−40 to 158° F)
Humidity	Up to 90%, noncondensing

1.2.4 DATA TRANSLATION FORMATS

Table 1-2 lists the data translation formats available on the 120A and 121A. Appendix A details each individual format.

Table 1-2. Data Translation Formats

Binary	ASCII-Hex SMS
DEC Binary	ASCII-Hex (Comma)
ASCII-BNPF	RCA Cosmac
ASCII-BHLF	Fairchild Fairbug
ASCII-B10F	MOS Technology
Spectrum	Motorola Exorciser
ASCII-Octal (Space)	Intel Intellec 8/MDS
ASCII-Octal (Percent)	Signetics Absolute Object
ASCII-Octal (Apostrophe)	Tektronix Hexadecimal
ASCII-Octal SMS	Texas Instruments SDSMAC
ASCII-HEX (Space)	Motorola Exormax
ASCII-Hex (Percent)	Hewlett-Packard 64000 Absolute
ASCII-Hex (Apostrophe)	Intel MCS-86 Hexadecimal Object

1.3 PROGRAMMER CONFIGURATIONS

The programmer includes remote control and serial I/O capability using any of 26 data translation formats available (see Table 1-2.) Table 1-3 lists the configurations of both the 120A and 121A.

Table 1-3. 120A and 121A Configurations

PART NUMBER	RAM SIZE	POWER CORD
120A	64K x 8	United States
	32K x 8	United States
	64K x 8	European
	32K x 8	European
121A	256K x 8	United States
	128K x 8	United States
	256K x 8	European
	128K x 8	European

1.4 CALIBRATION

Calibration of your programmer is normally unnecessary. This is because high-precision components keep your programmer within specification.

However, you may wish to calibrate your machine if:

- Your company policy requires periodic calibration.
- You replace a high-precision component; or if
- You are not receiving the proper programming yields. In this case, complete the troubleshooting procedure in Section 4 first. If you find, after completing the procedure, that your problem still persists, refer to Section 5 - Calibration.

1.5 FIELD APPLICATIONS SUPPORT

Data I/O has Field Applications Engineers (FAEs) throughout the world who can provide you additional information about interfacing Data I/O products with other equipment or answer your questions about problems you may have with your equipment.

The locations of the FAEs within the United States are given on the address list at the back of this manual. Call your regional FAE if you have any questions or problems. For international applications support, contact your nearest Data I/O Service Center.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period is one year and begins when you receive the programmer.

The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Service Center.

1.7 SERVICE

Data I/O maintains Service Centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. A list of all the Service Centers is located at the back of this manual.

1.8 ORDERING

To place an order for equipment, contact your Data I/O sales representative.

Orders for shipment must include the following:

- Description of the equipment. (See the latest Data I/O Price List or contact your sales representative for equipment and part numbers.)
- Purchase order number.
- Desired method of shipment.
- Quantity of each item ordered.
- Shipping and billing address of firm, including zip code.
- Name of person ordering the equipment.

Table 1-4. Programming Applications

ARRAY SIZE AND TECHNOLOGY	DEVICE PART NUMBER	FAMILY CODE	PINOUT CODE	LOGIC LEVEL
Advanced Micro Devices				
1024 x 8 MOS	2708/9708	21	27	VOL TS
2048 x 8 MOS	2716	19	23	VOL TS
4096 x 8 MOS	2732	19	24	VOL TS
4096 x 8 MOS	2732A	27	24	VOL TS
8192 x 8 MOS	2764(a)	AF	33	VOL TS
8192 x 8 MOS	2764A(a)	C1	33	VOL TS
16384 x 8 MOS	27128(a)	AF	51	VOL TS
16384 x 8 MOS	27128A(a)	C1	51	VOL TS
32768 x 8 MOS	27256(a)	C1	32	VOL TS
65536 x 8 MOS	27512(a)	DD	A4	VOL TS
Electronic Arrays				
1024 x 8 MOS	2708	21	27	VOL TS
2048 x 8 MOS	2716	19	23	VOL TS
Fairchild SemiConductor				
1024 x 8 MOS	2708	21	27	VOL TS
Fujitsu				
1024 x 8 MOS	8518 (2708)	21	27	VOL TS
2048 x 8 MOS	8516 (2716)	19	23	VOL TS
4096 x 8 MOS	2732A	27	24	VOL TS
4096 x 8 MOS	2732A-35	27	24	VOL TS
4096 x 8 MOS	8532 (2732)	19	24	VOL TS
8192 x 8 MOS	2764	45	33	VOL TS
8192 x 8 CMOS	27C64	45	33	VOL TS
16384 x 8 MOS	27128(a)	45	51	VOL TS
16384 x 8 CMOS	27C128(a)	45	51	VOL TS
32768 x 8 MOS	27256(a)	45	32	VOL TS
32768 x 8 CMOS	27C256(a)	45	32	VOL TS
Hitachi				
2048 x 8 MOS	482716	19	23	VOL TS
2048 x 8 MOS (EE)	48016	33	23	VOL TS
4096 x 8 MOS	482532	19	25	VOL TS
4096 x 8 MOS	482732	19	24	VOL TS
4096 x 8 MOS	482732A	27	24	VOL TS
4096 x 8 MOS	482732P	19	24	VOL TS
8192 x 8 MOS	482764	35	33	VOL TS
Intel				
512 x 8 MOS	2704/8704	21	26	VOL TS
1024 x 8 MOS	2708/8708	21	27	VOL TS
1024 x 8 MOS	2758	19	22	VOL TS
1024 x 8 MOS	2758S1865	19	35	VOL TS
2048 x 8 MOS	2716	19	23	VOL TS
2048 x 8 MOS	2815	85	23	VOL TS
2048 x 8 MOS (EE)	2816	37	23	VOL TS
2048 x 8 MOS (EE)	2816A(a)	A5	96	VOL TS
2048 x 8 MOS (EE)	2817A(a)(c)	BF	A2	VOL TS
4096 x 8 MOS	2732	19	24	VOL TS
4096 x 8 MOS	2732A(a)	27	24	VOL TS
8192 x 8 MOS	2764(a)	79	33	VOL TS
8192 x 8 MOS	2764A(a)	93	33	VOL TS
8192 x 8 MOS (EE)	2864(a)	A5	98	VOL TS
16384 x 8 MOS	27128(a)	79	51	VOL TS
16384 x 8 MOS	27128A(a)	93	51	VOL TS
32768 x 8 MOS	27256(a)	93	32	VOL TS
Mitsubishi				
1024 x 8 MOS	2708	21	27	VOL TS
1024 x 8 MOS	58732S(2708)	21	27	VOL TS
2048 x 8 MOS	2716	19	23	VOL TS
4096 x 8 MOS	2732	19	24	VOL TS
8192 x 8 MOS	2764	35	33	VOL TS
Mostek				
2048 x 8 MOS	2716	19	23	VOL TS
Motorola				
1024 x 8 MOS	68708/2708L	21	27	VOL TS
2048 x 8 MOS (EE)	2816	43	23	VOL TS
2048 x 8 MOS	MCM 2716	19	23	VOL TS
2048 x 8 MOS	TMS2716	23	28	VOL TS
096 x 8 MOS	68732-0	25	44	VOL TS
4096 x 8 MOS	68732-1	25	45	VOL TS
4096 x 8 MOS	MCM 2532	19	25	VOL TS
8192 x 8 MOS	68764	25	29	VOL TS
8192 x 8 MOS	68766	25	29	VOL TS
National Semiconductor				
1024 x 8 MOS	2708	21	27	VOL TS
1024 x 8 MOS	2758A	19	22	VOL TS
1024 x 8 MOS	2758B	19	35	VOL TS
2048 x 8 MOS	2716	19	23	VOL TS
2048 x 8 CMOS	27C16	19	23	VOL TS
2048 x 8 MOS (EE)	2816	37	23	VOL TS
2048 x 8 MOS (EE)	9716	B3	23	VOL TS
4096 x 8 MOS	2532	19	25	VOL TS
4096 x 8 MOS	2732	19	24	VOL TS
4096 x 8 CMOS	27C32H	BD	24	VOL TS
8192 x 8 MOS	2764H	63	33	VOL TS

Table 1-4. Programming Applications (Continued)

ARRAY SIZE AND TECHNOLOGY	DEVICE PART NUMBER	FAMILY CODE	PINOUT CODE	LOGIC LEVEL
	NEC			
2048 x 8 MOS	2716	19	23	VOL TS
4096 x 8 MOS	2732	19	24	VOL TS
4096 x 8 MOS	2732A	27	24	VOL TS
8192 x 8 MOS	2764	79	33	VOL TS
	OKI			
1024 x 8 MOS	2708	21	27	VOL TS
1024 x 8 MOS	2758	19	22	VOL TS
2048 x 8 MOS	2716	19	23	VOL TS
4096 x 8 MOS	2532	19	25	VOL TS
4096 x 8 MOS	2732	19	24	VOL TS
	Ricoh			
4096 x 8 MOS	RD5H32	27	24	VOL TS
8192 x 8 MOS	RD5H64	25	29	VOL TS
	SEEQ			
2048 x 8 MOS (EE)	5213[a][b]	A5	96	VOL TS
2048 x 8 MOS (EE)	52B13[a][b]	A5	96	VOL TS
2048 x 8 MOS (EE)	5213H[a][b]	B9	96	VOL TS
2048 x 8 MOS (EE)	52B13H[a][b]	B9	96	VOL TS
4096 x 8 MOS (EE)	52B23[a]	AB	97	VOL TS
4096 x 8 MOS (EE)	52B23H[a]	AB	97	VOL TS
8192 x 8 MOS (EE)	52B33[a]	AB	98	VOL TS
8192 x 8 MOS (EE)	52B33H[a]	AB	98	VOL TS
8192 x 8 MOS	5133[a]	35	33	VOL TS
8192 x 8 MOS	5133H[a]	35	33	VOL TS
16384 x 8 MOS	5143[a]	79	51	VOL TS
16384 x 8 MOS	5143H[a]	79	51	VOL TS
	Synertek			
2048 x 8 MOS	2716	19	23	VOL TS
	Texas Instruments			
1024 x 8 MOS	2508	19	22	VOL TS
1024 x 8 MOS	2708/27L08	21	27	VOL TS
2048 x 8 MOS	2516	31	23	VOL TS
2048 x 8 MOS	2716	23	28	VOL TS
4096 x 8 MOS	2532	31	25	VOL TS
4096 x 8 MOS	25L32	19	25	VOL TS
4096 x 8 MOS	2732	31	24	VOL TS
8192 x 8 MOS	2564	31	30	VOL TS
	Toshiba			
512 x 8 MOS	321 (2704)	21	26	VOL TS
1024 x 8 MOS	322 (2708)	21	27	VOL TS
2048 x 8 MOS	323 (2716 1V)	19	23	VOL TS
4096 x 8 MOS	2732D	19	24	VOL TS
	Xicor			
512 x 8 MOS (EE)	2804	37	82	VOL TS
2048 x 8 MOS (EE)	2816	37	23	VOL TS
8192 x 8 MOS (EE)	2864	C3	98	VOL TS

[a] The device can be programmed in the electronic identifier mode. To select this mode, enter family code FF and pinout code FF. The programmer will automatically select the correct family and pinout codes.

[b] CAUTION: Family/pinout FF/FF cannot be used in verifying or loading of these devices due to possible erasing of device or byte.

[c] CAUTION: Programmer does not check if device is inserted backwards. Device can be destroyed if inserted backwards during any device operation.

SECTION 2
INSTALLATION

2.1 INTRODUCTION

The following sections present information necessary for setting up your programmer for operation. Included are power source connection, power and fuse requirements, and connecting a Data I/O Data Control Unit (DCU) or other peripheral.

2.2 INSPECTION

Your programmer was thoroughly tested and inspected before shipment. The unit was carefully packaged to prevent damage and should arrive free of any defects and in perfect operating condition. For troublefree operation, verify upon receipt that the equipment listed in Table 2-1 is present. Carefully inspect it for any damage that may have occurred during transit. If you note any damage, file a claim with the carrier and notify Data I/O. Check the operation only after completing the installation procedures in sections 2.3 through 2.4.

If you wish, keep the box and its packing material for future shipment.

2.3 POWER CONNECTION

The following paragraphs explain the procedures for connecting the programmer to a power source.

Table 2-1. Required Equipment.

DESCRIPTION	QTY.	DATA I/O PART NUMBER
Programmer		
120A or	1	990-0120-XXX*
121A	1	990-0121-XXX*
Power Cord		
United States or	1	401-1577
Europe	1	416-0010
Instruction Manual	1	10-990-0120-002
Operator's Guide		
120A or	1	12-990-0120-002
121A	1	12-990-0121-002

*XXX - will vary with voltage and RAM size.

2.3.1 CHECKING THE OPERATING VOLTAGE

CAUTION

Do not operate the unit at voltages outside the factory-selected range or you will damage the programmer and any device in it.

The factory has selected the proper voltage according to your specification (see label on rear panel). The unit will operate when the line voltage is within +5%/—10% of the voltage shown on the voltage selection card. The card is connected to the AC power connector at the rear of the unit. Refer to Figure 2-1. If the two do not match (label and card), change the voltage selection card according to the instructions in Section 2.3.2.

WARNING

Do not insert anything other than the voltage selection card into the slot, or you will create a shock hazard. The inserted end of the card connects raw line voltage to the power supply transformer.

2.3.2 GROUNDING THE UNIT

WARNING

Failure to ground the programmer may create a shock hazard. Do not defeat the 3-wire grounding cord by using extension cords or adapters.

To remove or install the line fuse and change the line voltage selection (Refer to Figure 2-1):

1. Disconnect the power cord.
2. Slide the plastic cover to expose the voltage selection card.
3. Remove the line fuse by pulling on the "FUSE PULL" tab.
4. Pull out the card.
5. Replace the card so that the correct line voltage is displayed when the card is installed. Reinstall the line fuse.

The power cord contains three conductors. When the cord is connected to a 3-wire AC power system, the ground connector grounds the programmer's chassis, eliminating shock hazards. **Do not use anything, such as a 2-conductor extension cord, that would break contact between the programmer and an earth ground.**

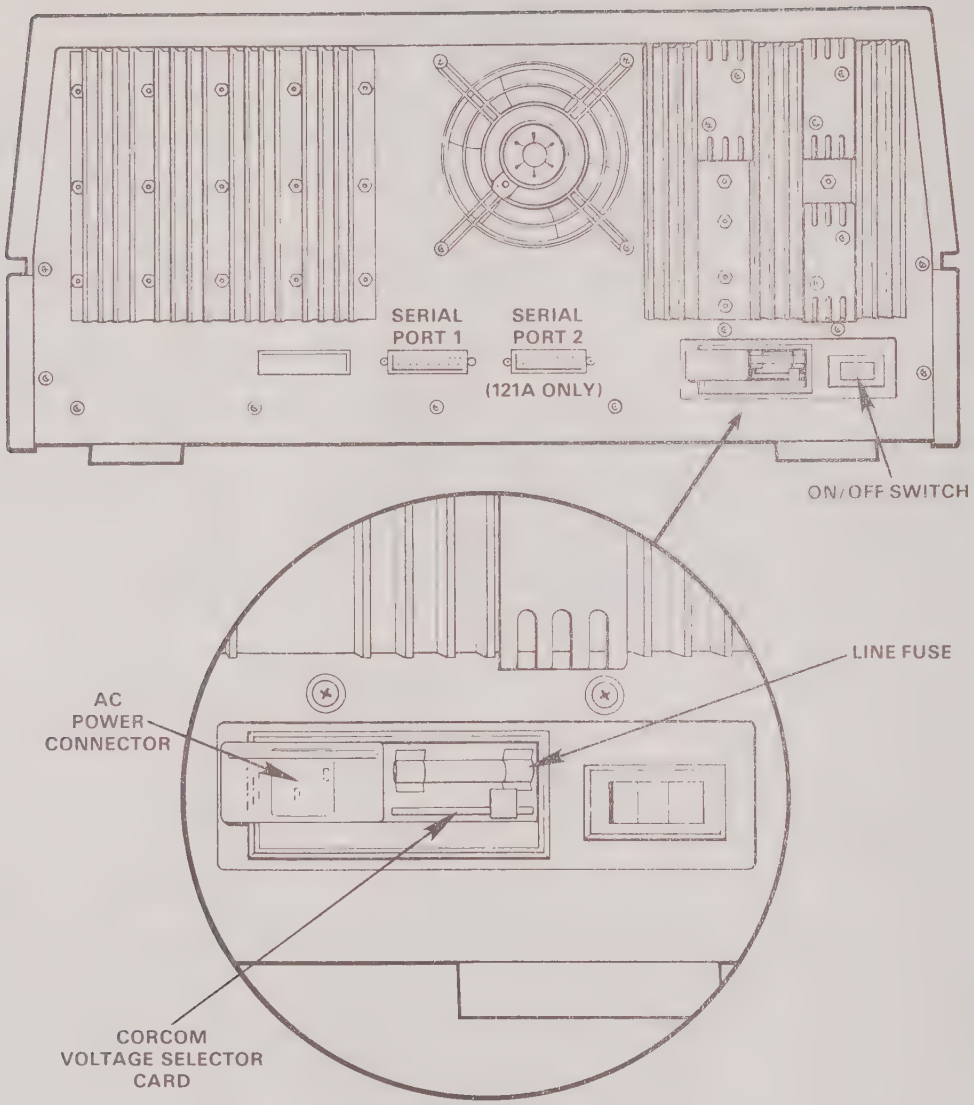


Figure 2-1. Rear Panel

2.3.3 FUSE ACCESS

The programmer's line fuse is located on the rear panel, as shown in Figure 2-1. Table 2-2 gives the fuse ratings for each operating voltage.

To access the AC line fuse, execute the following steps while referring to Figure 2-1.

1. Disconnect the power cord.
2. Slide the plastic cover to expose the line fuse.
3. Remove the line fuse by pulling on the "FUSE PULL" tab.

To access the eight power supply fuses, F1 through F8, on the Power Supply Bridge Board (P/N 702-1645), first remove the unit's top cover as shown in Figure 2-2. The power Supply Bridge Board is located next to the large filter capacitors. Figure 2-3 is a map of the power supply fuses and their ratings. The fuses will snap in and out of their holders without tools.

2.4 THE SERIAL INTERFACE

An RS232C and 20mA current loop serial interface is used to connect the programmer to computer systems, the DCU, and other peripherals. The following paragraphs describe the procedures for cabling and setting parameters when interfacing the programmer with other equipment.

Table 2-2. Line Fuse Ratings

OPERATING VOLTAGE	LINE FUSE
100 VAC	3 amp slow-blow
120 VAC	3 amp slow-blow
220 VAC	2 amp slow-blow
240 VAC	2 amp slow-blow

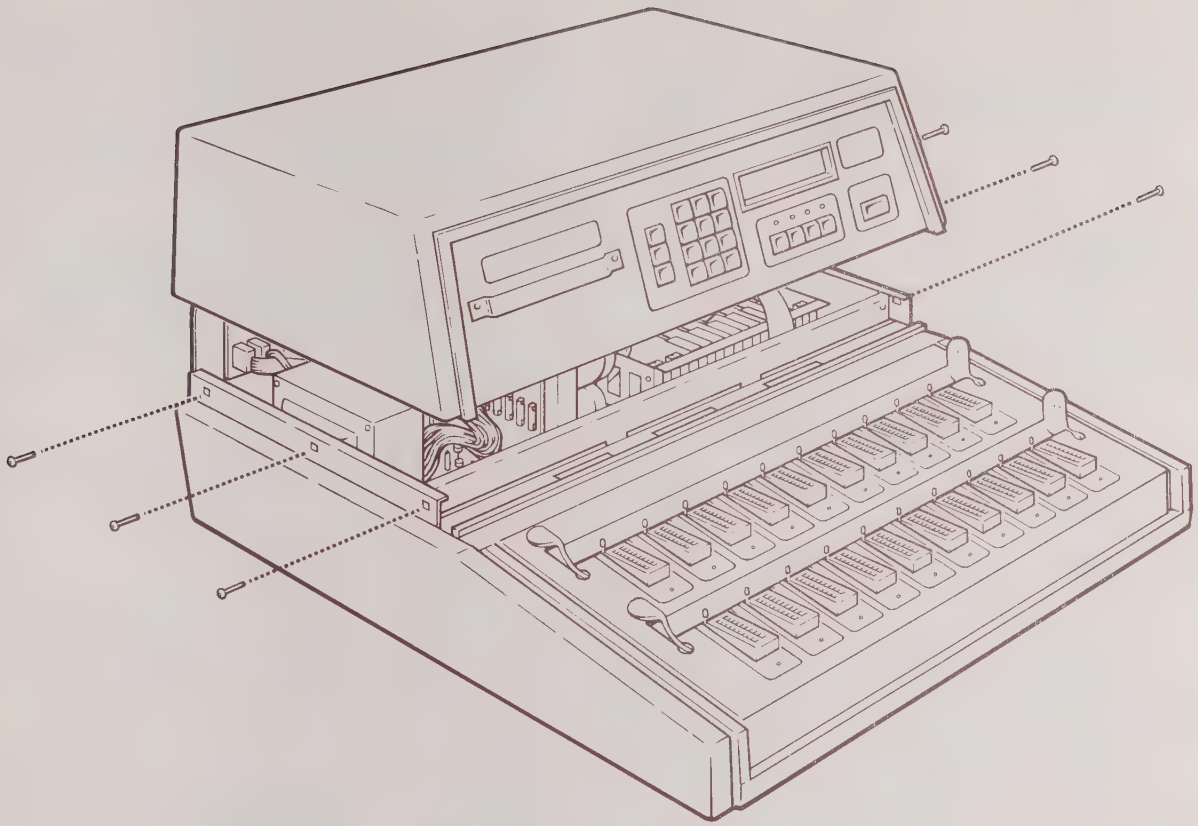


Figure 2-2. Removing the Top Cover

F1 = 2 amp slow blow
F2 = 2 amp slow blow
F3 = 1 amp slow blow
F4 = 1 amp slow blow
F5 = 10 amp
F6 = 10 amp
F7 = 8 amp
F8 = 8 amp

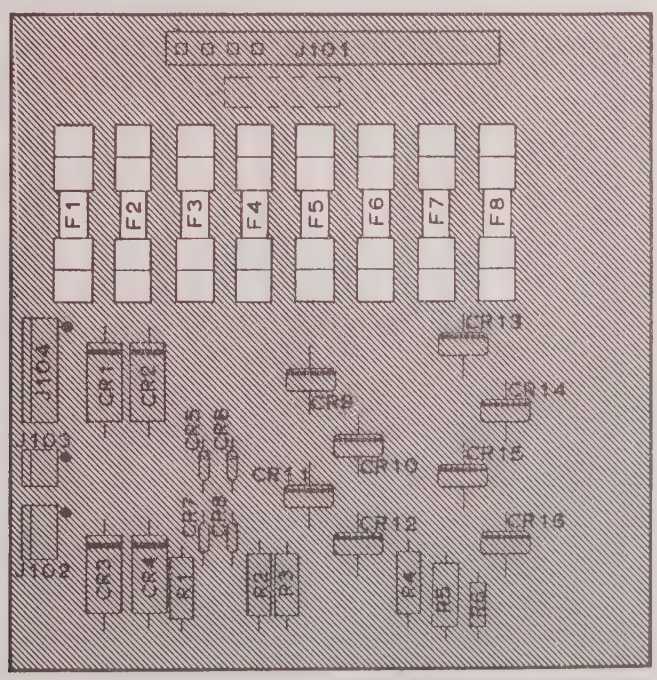


Figure 2-3. Power Supply Bridge Board

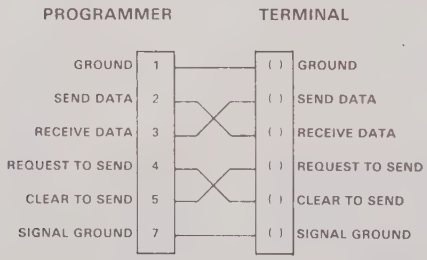
2.4.1 CABLING

To connect the programmer to other equipment, follow the RS232C or 20 mA current loop specifications given in Table 2-3. The 121A serial ports have the same connector pin assignments. Figure 2-4 shows sample inter-connection methods.

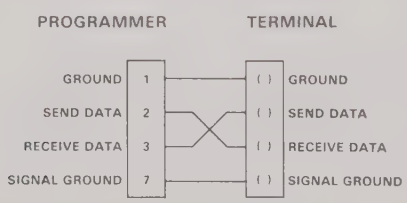
Table 2-3. Serial Interface Connector Pin Assignment

PIN NO.	SIGNAL MNEMONIC	DESCRIPTION
1	Ground	In the RS232C environment this line is common for the −12V and provides a safety ground connection to the RS232C-compatible terminal. In the TTY environment, the −12V VDC signal line provides the signal return for a TTY terminal.
2	Send Data	Transmits data at RS232C voltage levels (+12 and −5V.)
3	Receive Data	Accepts data at RS232C voltage levels.
4	Request To Send	This line is normally held high by the programmer. It is dropped to inhibit data transmission from a remote source.
5	Clear to Send*	A high level on this line allows the programmer to transfer data. A low level inhibits data transfer.
6	Data Set Ready	Connected by internal jumper to Data Ready (pin 20.)
7	Signal Ground	This line provides a common signal connection to the RS232C remote source.
8	Carrier Detect*	This line is positive when modem detects a carrier signal. This line is sampled by the programmer if used.
9		Not used.
10		Not used.
11	20 mA Send	Transmits data using active 20 mA current loop.
12	20 mA Receive	Accepts data using active 20 mA current loop.
13	Detect	20 mA Receive Data on pin 12 is internally converted to RS232C levels. Output on pin 13 should be jumpered externally to Receive Data, pin 3.
14-19		Not used.
20	Data Ready	Connected by internal jumper to Data Set Ready, pin 6. A high level on this line from the RS232C data terminal indicates that the data terminal is ready.
21-25		Not used.

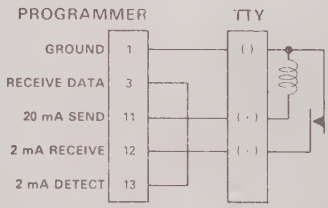
*Pins 5 and 8 have internal pull-ups and need no connection if unused.



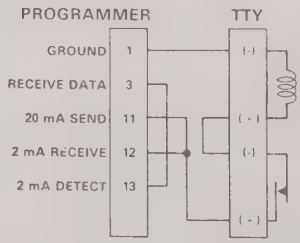
a) RS232C Connection Half/Full Duplex with Handshake



b) RS232C Connection Half/Full Duplex without Handshake



c) 20 mA Current Loop Connection, Full Duplex



d) 20 mA Current Loop Connection, Half Duplex

Figure 2-4. Sample Interconnection Methods

2.4.2 Setting Parameters

Four switch assemblies are used for setting parameters for I/O operations. They are described in table 2-4. Figure 2-5 shows the location of each card in the card cage. The following paragraphs describe the settings for each of these switch assemblies. Figures 2-6 through 2-8 show the actual switch assemblies and their settings.

Table 2-4. Switches for Setting I/O Parameters

SWITCH	LOCATION	FUNCTION
U3	Specific I/O Card (Figure 2-6)	Sets a default device for Load, Program, **Set Program (121A)**, and Verify operations. The programmer will load, program or verify the chosen default device. See table 2-5 and figure 2-6.
U4	Specific I/O Card (Figure 2-6)	Sets various operating parameters. —Segment 8 - DCU. Must remain off if DCU is not hooked up. —Segment 7 - Data Lock. Must remain off if not in use. —Segment 6 - Troubleshooting. Must remain off if not using Select Function 12. —Segment 5 - Ports. Off for 120A. **Switch on for 121A. If left off on 121A, input from port #2 is ignored.** —Segment 4 - RTS. Off, handshake lines only active during I/O operations. On, I/O always active. —Segment 3 - Electronic ID. Must remain off to permit electronic identification. When on, electronic identification is inhibited. —Segment 2 - Auto remote mode. When on, the programmer will power up in remote control. —Segment 1 - Must remain off.
U1	Keyboard Display and Serial I/O Card (Figure 2-7)	Sets baud rate. —Turn segment on for desired baud rate. All other segments must remain off.
U2	Keyboard Display and Serial I/O Card (Figure 2-7)	Sets stop bits and parity. —Segment 1 - Stop bits (off = 2), (on = 1) —Segment 2 - Parity - off/on. —Segment 3 - Parity - (off = odd) or (on = even) —Segment 4 - Must remain off.
U3	Dual Serial Board **(121A Only)** (Figure 2-8)	Set baud rate. —Turn segment on for desired baud rate. All other segments must remain off.
U4	Dual Serial Board **(121A Only)** (Figure 2-8)	Sets stop bits and parity. —Segment 4 - Parity (off = odd) and (on = even) —Segment 3 - Parity - off/on —Segment 2 - Stop bits (off = 2), (on = 1) —Segment 1 - Transparent inhibit. (off—enable)(on—inhibit)
U5	Dual Serial Board **(121A Only)** (Figure 2-8)	Not used. All segments must remain off.
U6	Dual Serial Board **(121A Only)** (Figure 2-8)	Not used. All segments must remain off.

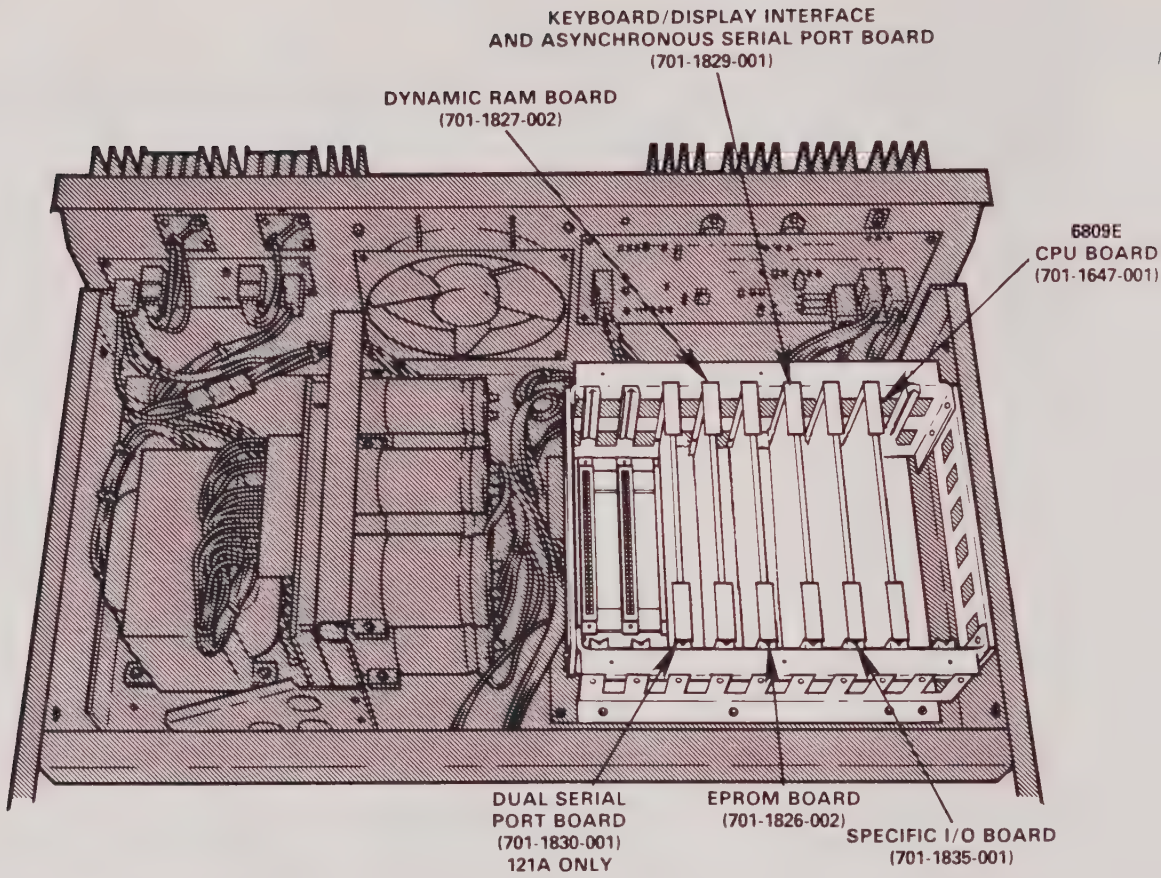


Figure 2-5. Top Internal View of the 120A and 121A

Parameter Switches on the Specific I/O Card

Figure 2-6 shows the specific I/O card and the two switch assemblies used for setting a default device and I/O parameters. Table 2-5 shows the binary values used for defining a default device. When the switch is set to zero, the programmer will prompt you for family and pinout codes. When a device is specified, it is not necessary for the operator to key in the family and pinout codes for programming that device.

The I/O switch assembly informs the programmer whether or not a DCU is interfaced, the data lock* is set, electronic ID is inhibited, the remote mode is automatically selected at power up, and the troubleshoot mode is activated. It also tells the programmer whether to accept commands from one or two serial ports. Finally, when the programmer is not hooked up to a peripheral, it determines whether or not the RTS line is active or inactive.

*Data lock is described in section 3.2.4.

Parameter Switches on the Keyboard Display and Serial I/O Card and Dual Serial Card (121A)

The switch assemblies on the Keyboard Display and Serial I/O card and the Dual Serial card are used to set the baud rate, parity, and stop bits as indicated in Figure 2-7 and 2-8. **The switch assembly on the Dual Serial card (121A) is used to set the baud rate, parity, and stop bits for serial port #2.**

2.4.3 INSTALLING THE DATA I/O DCU

If a DCU is used with the programmer, turn segment 8 on U4 to the ON position. It is located on the Specific I/O card and is indentified in Figure 2-6.

2.4.4 INHIBIT TRANSPARENT I/O

The 121A passes all data received from one port to the other. This transparency feature can be inhibited (permitting independent operation of the two ports) by placing segment 1 of U4, on the dual serial board, in the ON position.

2.5 REPACKAGING FOR SHIPMENT

If the instrument is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identify the owner. In correspondence, identify the unit by serial number, mode number and name.

If you use the original shipping container, place the instrument in the container with appropriate packing material and seal the container with strong tape. If you use some other container, be sure that it is a heavy carton. Wrap it with heavy paper or plastic. Use the appropriate packing material and seal the carton with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

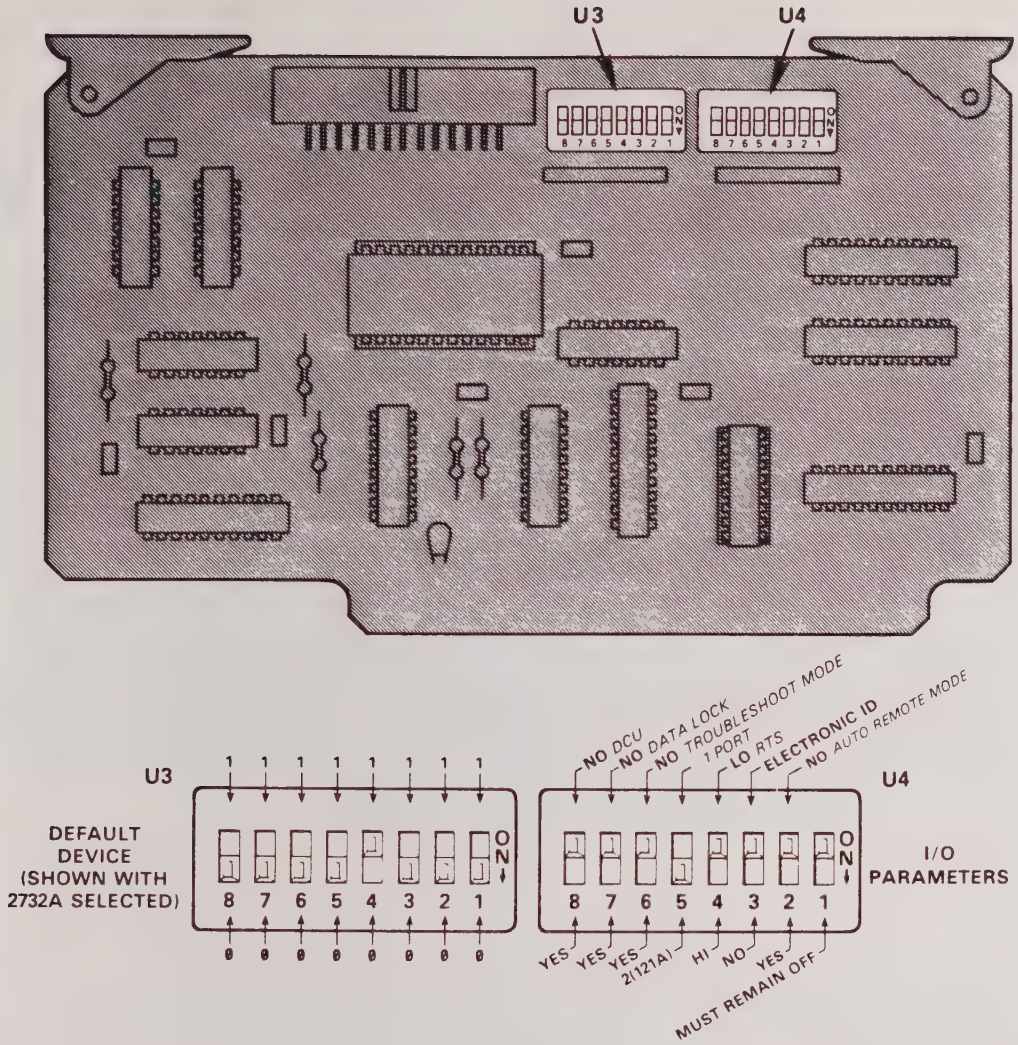


Figure 2-6. Setting Parameters on the Specific I/O Card

Table 2-5. Binary Values for Setting Default Devices[1]

DEVICE	BINARY VALUE[2]	EQUIVALENT CODES	
		Family Code	Pinout Code
	Segment: 87654321		
None	00000000	N/A	N/A
2704, 321	00000001	21	26
2708, 8518, 58732S, 68708, 27L08, 322	00000010	21	27
2716 (3 voltage)	00000011	23	28
2508, 2758, 2758A	00000100	19	22
2758/S1865, 27C58, 2758B	00000101	19	35
462716, 8516, 4716, 2516, 27C16, 323 single voltage 2716	00000110	19	23
462732, 8532, 2732, 2732D, 27C32	00000111	19	24
2732A	00001000	27	24
462532, 2532, 65C32	00001001	19	25
68732-0	00001010	25	44
68732-1	00001011	25	45
68764, 68766	00001100	25	29

Table 2-5. Binary Values for Setting Default Devices[1] (Continued)

DEVICE	BINARY VALUE[1] Segment: 87654321	EQUIVALENT CODES Family Code	Pinout Code
Intel 2764, 462764	00001101	35	33
Texas Instruments (T.I.) 2564	00001110	31	30
Motorola 2816 EE	00010000	43	23
Hitachi 48016EE	00010001	33	23
Intel 2816EE	00010010	37	23
National 2764H	00010011	63	33
Intel 27128	00010100	35	51
Intel 2764 (Intelligent Algorithm)	00011000	79	33
T.I. 2516 (Fast Algorithm)	00011001	31	23
T.I. 2532 (Fast Algorithm)	00011010	31	25
Intel 27128 (Intelligent Algorithm)	00011011	79	51
Intel 2815	00011100	85	23
Intel 27256	00011101	93	32
SEEQ 5211	00011111	A5	23
Intel 2764A (Intelligent Algorithm)	00100001	93	33
Intel 27128A (Intelligent Algorithm)	00100010	93	51
Intel 2816AEE	00100100	A5	96
Intel 2817AEE	00100101	BF	A2
Intel 2864EE	00100110	A5	98
National 27C32H	00100111	BD	24
National 9716	00101000	B3	23
AMD 2764	00101001	AF	33
AMD 27128	00101010	AF	51
AMD 2764A	00101011	C1	33
AMD 27128A	00101100	C1	51
AMD 27256	00101101	C1	32
AMD 27512	00101110	DD	A4
Fujitsu 2764, 27C64	00101111	45	33
Fujitsu 27128, 27C128	00110000	45	51
Fujitsu 27256, 27C256	00110001	45	32
SEEQ 52B23, 52B23H	00110010	AB	97
SEEQ 52B33, 52B33H	00110011	AB	98
T.I. 2732	00110100	31	24
Xicor 2804	00110101	37	82
SEEQ 5213H, 52B13H	00110110	B9	96
Xicor 2864	00110111	C3	98
T.I. 2732A	00111000	63	24
T.I. 2716	00111001	BD	23
T.I. 2532	00111010	BD	25
T.I. 2564	00111011	BD	30
Electronic ID	11111111	FF	FF

[1]Note: The default device selected can be verified from the front panel by pressing SELECT, entering 10 (configuraton number) and pressing the Shift 3 key.

[2]0 = Segment is in the ON position.
1 = Segment is in the OFF position.

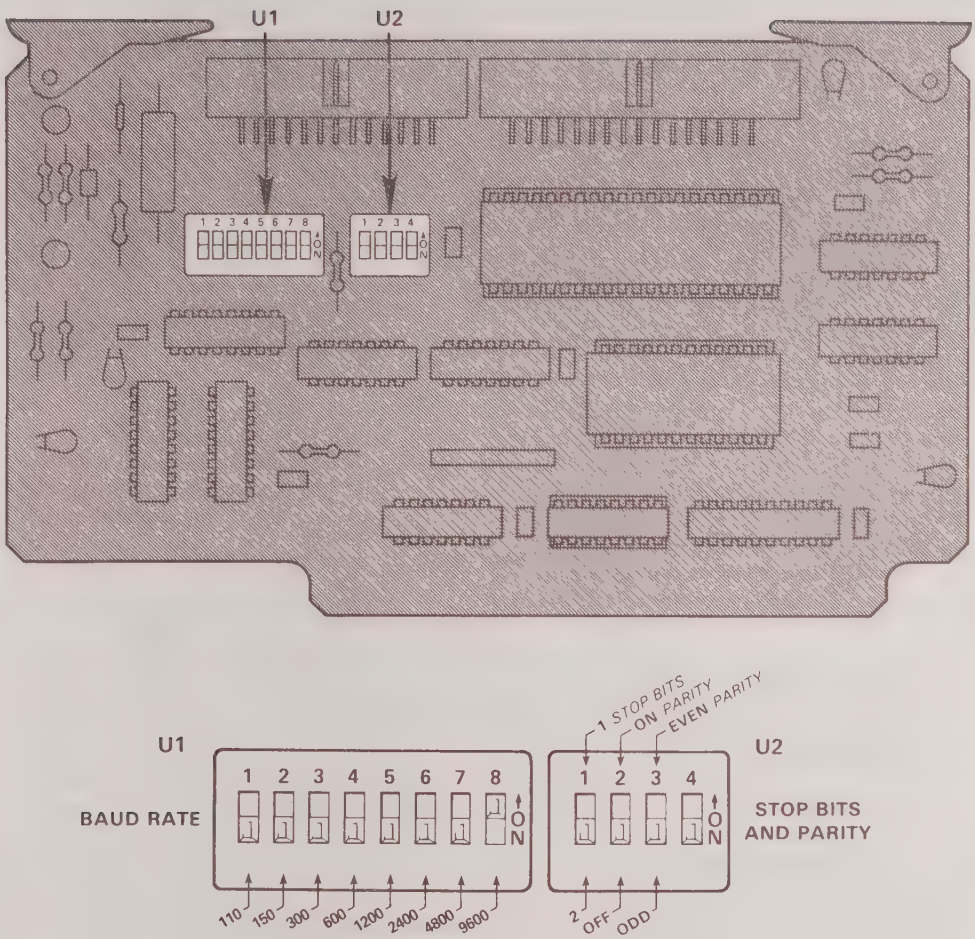


Figure 2-7. Keyboard Display and Serial I/O Card

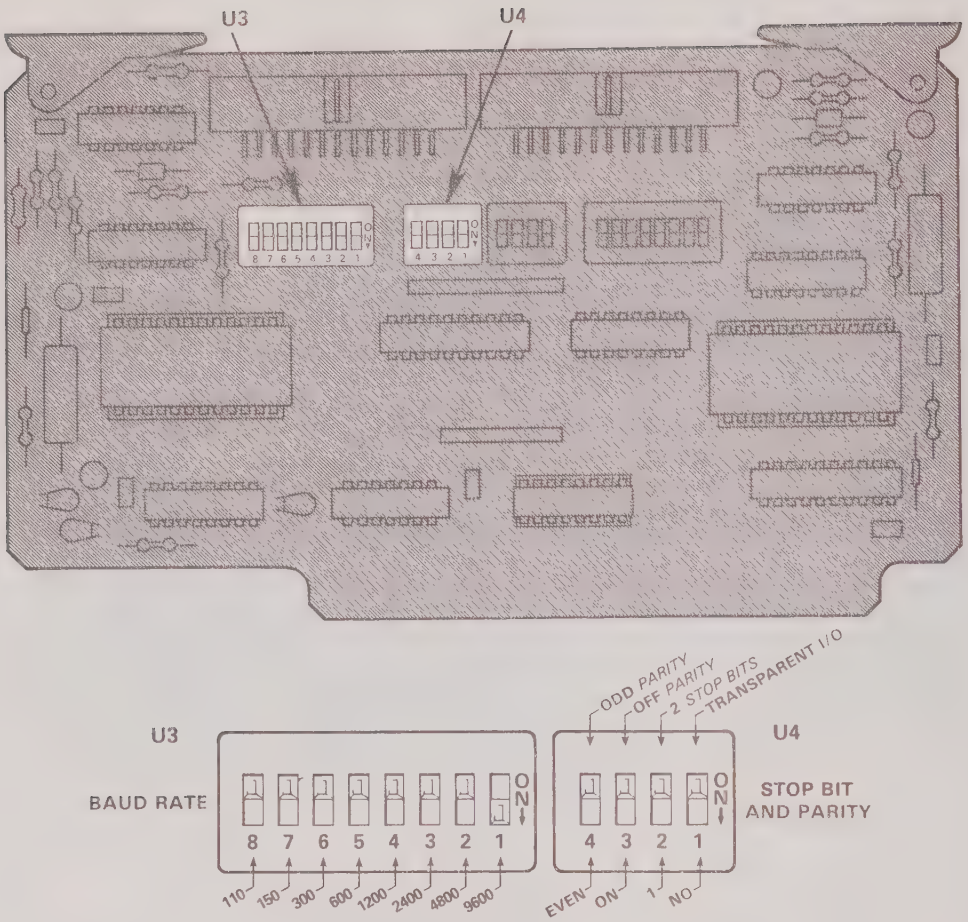


Figure 2-8. Dual Serial Card (121A only)

SECTION 3
OPERATION

3.1 INTRODUCTION

This section contains operating descriptions and procedures for using either the 120A or 121A Gang Programmer as a stand-alone unit, with a peripheral data storage instrument such as a Data Control Unit (DCU), and in remote control.

3.1.1 OVERVIEW

All data communications occur between the programmer's internal RAM and the serial port or the devices in the sockets. The following defines the possible operations:

- A data transfer from one device (120A/121A) or multiple devices (121A only) to the programmer RAM is a **Load from Part(s)** operation.
- A data transfer from the serial port to the programmer RAM is a Load from Port operation.
- A data transfer from the programmer RAM to a device or devices is a Program or **Set Program operation (121A only)**. When devices are programmed, they are automatically verified as well.
- A data transfer from the programmer RAM to the serial port is a Send to Port operation (Select Function 08).
- A byte-by-byte comparison of the data in RAM with the data in a programmed device is a Verify or **Set Verify operation (121A only)**.
- RAM data can be manipulated and parameters set using Select Functions.

Detailed descriptions of the operations follow.

LOAD FROM PART(S). A Load from Part(s) operation consists of transferring data from one or more master devices to the programmer RAM. When the data transfer is complete, the programmer calculates the sum-check (a 16-bit summation of binary data expressed as four hexadecimal characters) of the loaded data and displays it.

LOAD FROM PORT. In a Load from Port operation, data from the serial port is transferred to the programmer RAM. When completed, the programmer calculates the sum-check of the data. If a sum-check has been sent with the data from the serial port, the programmer will compare the two and signal an error if they do not match.

PROGRAM. Two methods of programming follow. **Both methods are available in the 121A. Set Programming is not available on the 120A.**

- Program Parts. A program operation duplicates data in the programmer RAM into each installed device. Data is programmed one byte at a time simultaneously into each device. After the devices are programmed, the device data and corresponding RAM data are compared or "verified" automatically to check that they are identical.
- **Set Programming (121A only)**. A set program operation duplicates the data in the programmer RAM into sets of devices. The RAM is partitioned into data blocks. Each block of data is programmed into a particular device in each set. Figure 3-1 provides a conceptual representation of set programming. The data from block A is programmed one byte at a time simultaneously into device "A" of each set. The other blocks follow: block B, block C, etc. Although the illustration shows sets of 5 PROMs, a set can be composed of as many as 20 PROMs (however only one set would be programmed at a time since there are only 20 sockets).

SEND TO PORT. In a Send to Port operation data from the programmer RAM is transferred to the serial port. You can instruct the programmer to send the data in any of the translation formats described in Appendix A.

VERIFY. A Verify is a byte-by-byte comparison between two sources of data. In a verify device or **Set Verify** operation, data from the device(s) in the sockets is compared byte-by-byte twice with the data in RAM. On the first pass, (first comparison), parametric checking is done by raising VCC within the manufacturer's specified range. On the second pass, the VCC value is lowered.

In a Verify from Port operation, incoming data from the serial port is compared byte-by-byte with the data in RAM.

SELECT FUNCTIONS. The SELECT key gives you access to additional functions used for changing the default values of parameters, manipulating RAM data, and accessing certain, less frequently used operations. See section 3.4 for a list of Select Functions, descriptions, and key sequences.

3.1.2 CONTROLS AND INDICATORS

Figure 3-2 and Table 3-1 show and describe the controls and indicators on the programmer.

NOTE

When the action symbol on the far right side of the display appears, the programmer is busy. At this time, only press keys to abort the operation.

3.1.3 PRELIMINARY INFORMATION ON USING THE OPERATION PROCEDURES IN THIS MANUAL

Section 3.4 describes Load, Program and Verify operations. Section 3.5 describes Select Functions and section 3.6 describes Remote Control. But before using the operation procedures in these sections, be sure that you read and understand sections 3.2 and 3.3.

Some basic assumptions are made in the operating procedures in this manual. The procedures assume that no errors occur. The programmer signals errors with three consecutive beeps. It also beeps if you press an incorrect key. When an error occurs, the display flashes the error message and the numeric code (only the code in remote

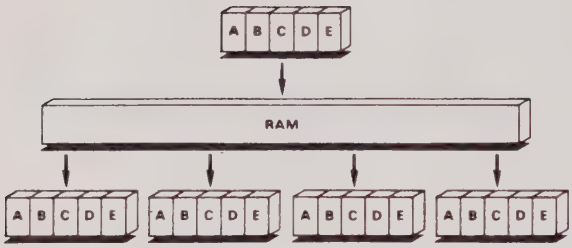


Figure 3-1. Set Programming on the 121A

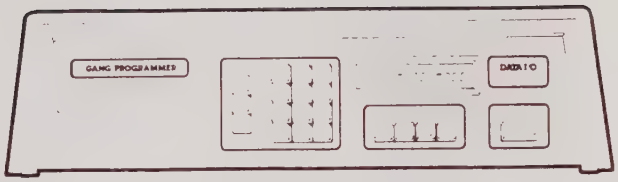


Figure 3-2. Front Panel

Table 3-1. Controls and Indicators

CONTROL/ INDICATOR	DESCRIPTION
POWER ON/OFF Switch	Located on the rear panel; applies or removes AC power.
SHIFT 1 key	Activates top letter on alphanumeric keys. After a Load, Program or Verify, pressing SHIFT 1 displays the Data Control Unit (DCU) program part number (file name.) This is available when the carat is in the display.
SHIFT 2 key	Activates center letter on alphanumeric keys. After a Load, Program or Verify, pressing SHIFT 2 displays program sum-check.* When in the DCU mode, the date of the program is also displayed.
SHIFT 3 key	Activates bottom letter on alpha-numeric keys. After a Program or Verify operation, pressing SHIFT 3 displays (left to right) illegal-bit errors, verify errors, and the number of successfully programmed parts. If Select Function 10 (Configuration Number) is displayed, pressing SHIFT 3 allows viewing of the Family and Pinout Codes in effect.
Alphanumeric Keys	Sends a number (no shift key pressed) or selected letter (depending on the shift key pressed) to memory and display.
CLEAR Key	Clears entered value to the left of <.
BACKSPACE Key	Clears character located to the left of <.
LOAD Key	Prepares programmer to load data into RAM.
Load indicator	Indicates Load mode is selected.
PROG Key	Prepares programmer to program device(s).
Program Indicator	Indicates Program mode is selected.
VERIFY Key	Prepares the programmer to compare RAM data with data from a master device, programmed devices, DCU file or other peripheral.
Verify Indicator	Indicates Verify mode has been selected.
SELECT Key	Prepares programmer to accept codes for Select Functions.
Select Indicator	Indicates Select mode has been chosen.
START Key	Commands the programmer to execute the function selected by the chosen mode key (LOAD, PROG, VERIFY or SELECT). Sends entered alphanumeric values and instructions to memory.
Display	Displays the current status of the programmer.

*The sum-check is for the first device in a set or for the block size. Pressing SHIFT 2 does not display the sum-check of all data in RAM or a file larger than the word limit, unless the Block Size is set. For a precise definition of sum-check, and how it relates to both the 120A and 121A Gang Programmers, see the Glossary (Table B-1).

control). Errors and corrective measures are described in section 3.7, Error Codes.

3.2 PREOPERATION PROCEDURES

CAUTION

Follow the procedures in this section carefully to avoid damaging the programmer or devices installed in it.

3.2.1 POWER-UP

The ON/OFF switch is located on the rear panel. When the programmer is first turned on, it will run through a self-test routine which checks the programmer's scratch RAM, firmware, data RAM and programming electronics, and then displays SELF TEST-OK. The programmer is now ready for operation.

CAUTION

Voltage transients during power-up and power-down can damage PROMs. Be sure that sockets are empty when switching power.

3.2.2 TESTS

The programmer performs a series of tests on each device before an operation is executed. The device tests are done in the following order.

1. Device Present. Confirms that a device has been inserted into a socket. A comparator monitors the voltage at pin 15. Inserting a part into the socket causes the voltage to change. This will notify the programmer that a device has been inserted.
2. Device Insertion. Checks to see that the device was inserted correctly and is not backwards or mis-justified in the socket.
3. Data Lines. Checks the devices' data lines for possible shorts. This is accomplished by alternating each line high while all other data lines are low. Once each data line has been pulled high, the test is complete.
4. Address Lines. Checks the devices' address lines for possible shorts. This is accomplished by alternating each line high while all other address lines are low. Once each address line has been pulled high, the test is complete.
5. Chip Select/Output Enable. Checks the devices' Chip Select and Output Enable lines. This is the final test that the programmer performs on the device after insertion. After the operator initiates a program operation, the programmer executes two more tests before it actually programs the part.
6. Illegal-Bit Test. Insures that any programmed bits are of the correct polarity. The test accomplishes this by verifying that the data in RAM could be programmed into the device even though there might already be programmed bits in the device.
7. Blank Check. The programmer makes sure that the device does not contain any programmed bits. (If the device is an EEPROM, is is automatically erased before this test. Non-blank parts may be programmed by pressing START again.

3.2.3 SETTING PARAMETERS

Before initiating any operations, certain parameters may need to be set via internal switches. These are described in Section 2 of this Manual.

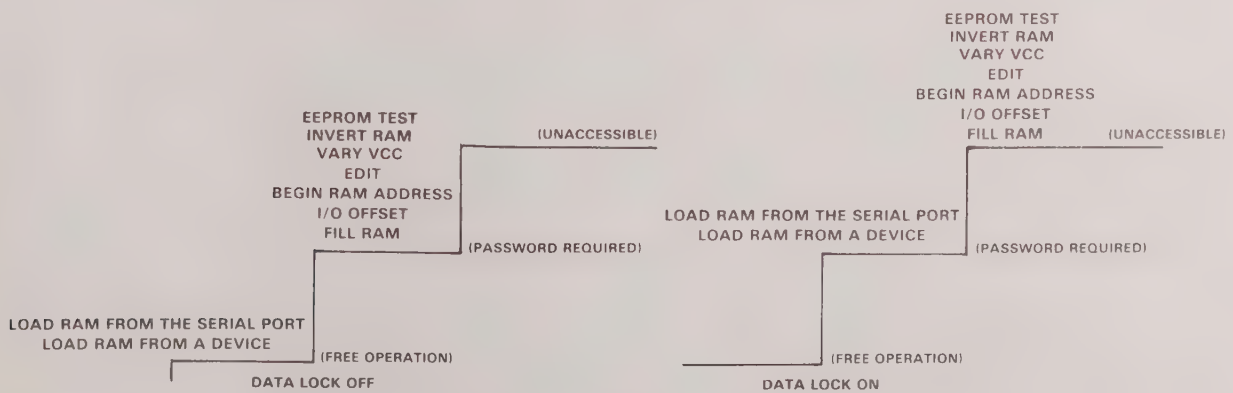
Some parameters are set via Select Functions. These are described in Section 3.5.

3.2.4 DATA LOCK AND PASSWORD

The Data Lock and Password allow you to protect your programming data in RAM against accidental changes that could cause misprogrammed parts.

The Data Lock controls the accessibility of certain functions, as shown in Figure 3-3. It is set via the Data Lock switch (see Figure 2-6). In the on position, all Load operations require a password and certain Select Functions (Edit, Block Limits, I/O Offset, Fill RAM, Vary VCC, Invert RAM and EEPROM Test) are totally inaccessible. In the off position, all load operations are freely accessible and these Select Functions require a password.

The Password consists of holding down the SHIFT 2 key while pressing BACKSPACE.



PASSWORD: Hold SHIFT 2 while pressing BACKSPACE

Figure 3-3. Data Lock

3.2.5 ELECTRONIC IDENTIFIER

The electronic identifier mode is selected by entering family code FF and pinout code FF. In this mode, the programmer can read and automatically set up the correct family and pinout codes for devices with electronic identifiers. The programmer sets up codes for the device in the lowest numbered socket, and then checks if all other devices inserted can be programmed with the same codes.

When family codes 27, 79 or 93 are entered, the programmer checks the installed devices with electronic identifiers and ensures that they can be programmed with the selected family and pinout codes. The electronic identifier feature can be disabled by setting a parameter switch (see Section 2.4.2) or using a select code (see Section 3.5).

3.3 INSERTING DEVICES

Care is necessary when inserting devices. The bottom pins of the device must be in the bottom pins of the socket. Also, be sure that pin 1 of the device is on top. Most PROMs have a notch or dot on the pin 1 end. (See Figure 3-4.)

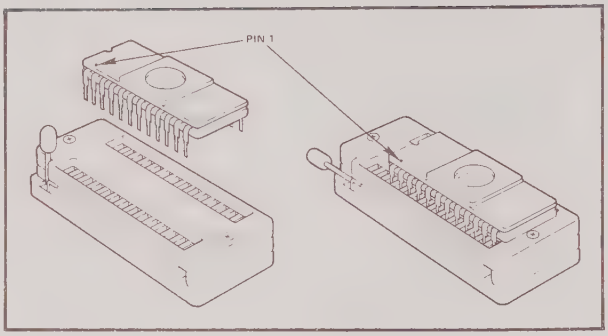


Figure 3-4. Correct Placement of PROMs in Socket

In a Load from Part operation, data must be loaded from socket 1 when loading data from a single device.

For more than one device, the devices are loaded consecutively into RAM, starting at socket 1 and going to socket 20. A representation of a multiple device load is provided in Figure 3-5.

Example:

Operator is loading 3 1K devices into a 121A with 32K of RAM.

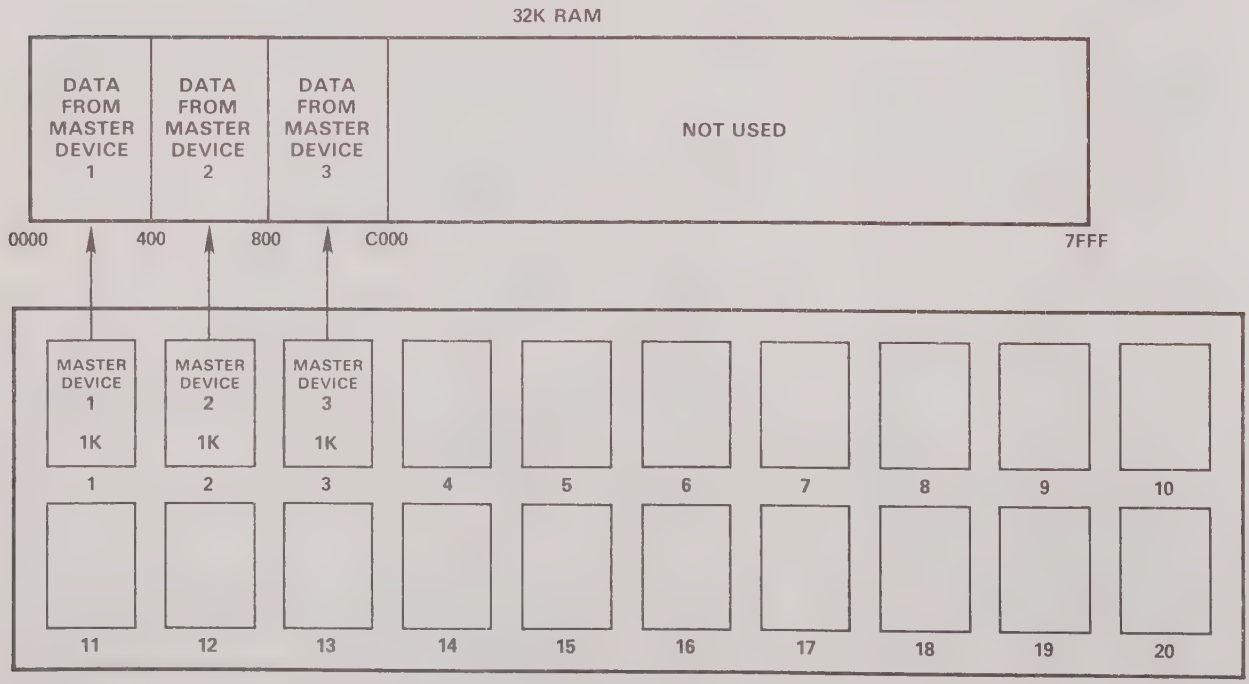


Figure 3-5. Multiple Device Load (121A Only)

3.4 OPERATIONS

Figures 3-6 through 3-12 illustrate operations accomplished with the LOAD, PROG, and VERIFY keys. Table 3-2 identifies and describes each operation. The illustrations for each operation include both a flowchart and a written procedure.

Table 3-2. Load, Program and Verify Operations

NAME	DESCRIPTION	FIGURE NUMBER
Load From Part(s)	Loads RAM from a programmed master device **or set of masters (121A) only.**	3-6
Load From Port/File	**Loads RAM from a DCU or other serial-transmitting data source.**	3-7
Program Parts	Programs devices from RAM data.	3-8
Set Programming	**Programs device sets from RAM data.**	3-9
Verify	Checks programmed devices for correct programming against the master data in the programmer RAM.	3-10
Set Verify	**Checks programmed device sets for correct programming against master data in the programmer RAM.**	3-11
Verify From Port/File	Checks RAM data against the master program whether it is from a DCU or other serial-transmitting source.	3-12

3.5 SELECT FUNCTIONS

Many of the programmer's operations are initiated by numeric Select Functions. These instruct the programmer's software to perform such tasks as RAM data manipulations, I/O functions, and miscellaneous utility operations.

Table 3-2 lists these operations and their numeric codes. Flowcharts which follow show the key sequence for each, except Select Function 12 - Troubleshooting. The Troubleshooting operation is discussed in Section 4, Troubleshooting.

Table 3-3. Select Functions

SELECT FUNCTION CODE	NAME	DESCRIPTION	DCU NECESSARY?	FIGURE NUMBER
01	Send to File	Send data in RAM (to word limit or block size) to DCU.	Yes	3-13
02	Copy File	Copies a specified file from disk 1 onto disk 2.	Yes	3-14
03	Delete File	Deletes a specified file from disk 1 on the DCU.	Yes	3-15
04	Copy Disk	Copies disk 1 of the DCU onto disk 2.	Yes	3-16
05	Format Disk	Formats disk 1 of the DCU **CAUTION** **Formatting takes approximately 5 minutes to execute. Do not attempt any front panel operations during formatting or the function will abort, resulting in an unformatted and unusable disk.**		3-17
06	Directory	Lists part numbers stored on disk. Press SHIFT 3 for Family/Pinout in effect. See Figure.	Yes	3-18
07	Free Space	Outputs the free space available on a disk.	Yes	3-19
08	Send to Port	Sends data in RAM (to word limit or block size) to the serial port.	No	3-20
09	Remote Mode	Puts the programmer under remote control.	No	3-21
10	Configuration Number	Displays the software configuration number (revision level) and RAM size.	No	3-22
11	Output Statistics	Programmer will send to port: I00 V00 0000 Illegal-Bit Errors ↑ ↑ ↑ Number of successfully programmed devices Verify Errors *NOTE* *These will be cleared (automatically set to 0) on completion of any LOAD operation (Load from Part, Port or File).*	No	3-23
12	Troubleshoot	Exercises various routines within the programmer to allow servicing. Refer to Section 4.	No	
13	Fill RAM	Fills RAM with the specified hex data.	No	3-24
14	I/O Offset	Selects the I/O address offset.	No	3-25
15	**Block Limits**	**121A only.** This select function sets the first RAM address from which data will move and the number of bytes that will be moved in an I/O or device operation. With the block size set less than or equal to the word limit of the device, the number of bytes moved will be equal to the block size times the number of devices in the set. The number of bytes moved will be equal to the block size, if the block size is greater than the device size. The default for the first address, and the number of bytes moved, are, respectively, zero and the device size times the set size. A zero block size will cause a default to the device word limit times the set size.	No	3-26
16	**Edit**	**121A only.** Allows editing of RAM data.	No	3-27
17	I/O Timeout	Disables the programmer's timeout.	No	3-28
18	**Vary VCC**	Allows the operator to test VCC levels over a specified range.	No	3-29
19	Invert RAM	Inverts data in RAM. (Changes ones to zeroes and zeroes to ones).	No	3-30
20	EEPROM Test	Allows the operator to functionally test EEPROM devices.	No	3-31
21	**View Sum-Check**	**121A only.** Allows the operator to view the sum-check of a particular device in a set	No	3-32

Table 3-3. Select Functions (Continued)

SELECT FUNCTION CODE	NAME	DESCRIPTION	DCU NECESSARY?	FIGURE NUMBER
22	**16-Bit Mode**	**121A only.** This mode allows the operator to convert the 121A into a 16-bit programmer. When this mode is in effect, the programmer will perform device related operations (Load, Program and Verify) as if each pair of 8-bit wide PROMs were a single 16-bit wide device. This mode can be used from either the front panel or in remote control.	No	3-32
23	**One or Two Pass Verify**	In a normal verify operation, programmed data in PROM is automatically verified twice against data in the programmer's RAM. This Select Function gives you the option of selecting the number of device verifications.	No	3-34
24	**View ID**	Allows the operator to view the electronic identifier of the installed device.	No	3-34
25	**Electronic ID**	Allows the operator to inhibit the electronic ID feature and/or the electronic ID warning message.	No	3-36

Use this procedure to load RAM form a programmed master device.

1. Insert device(s).
   You can insert and load more than one device (121A only).
2. Press LOAD.
   Display
   120A: LOAD FROM PART
   121A: LOAD FROM PARTS
3. Enter Password, if required.
4. Press START
   Display: F<
5. Enter Family and Pinout Codes. If correct codes are displayed continue with step 6.
6. Press START
   Display:
   120A: LOADING
   121A: LOADING
   Display: S* - XXXX (sum-check)
7. Remove devices.

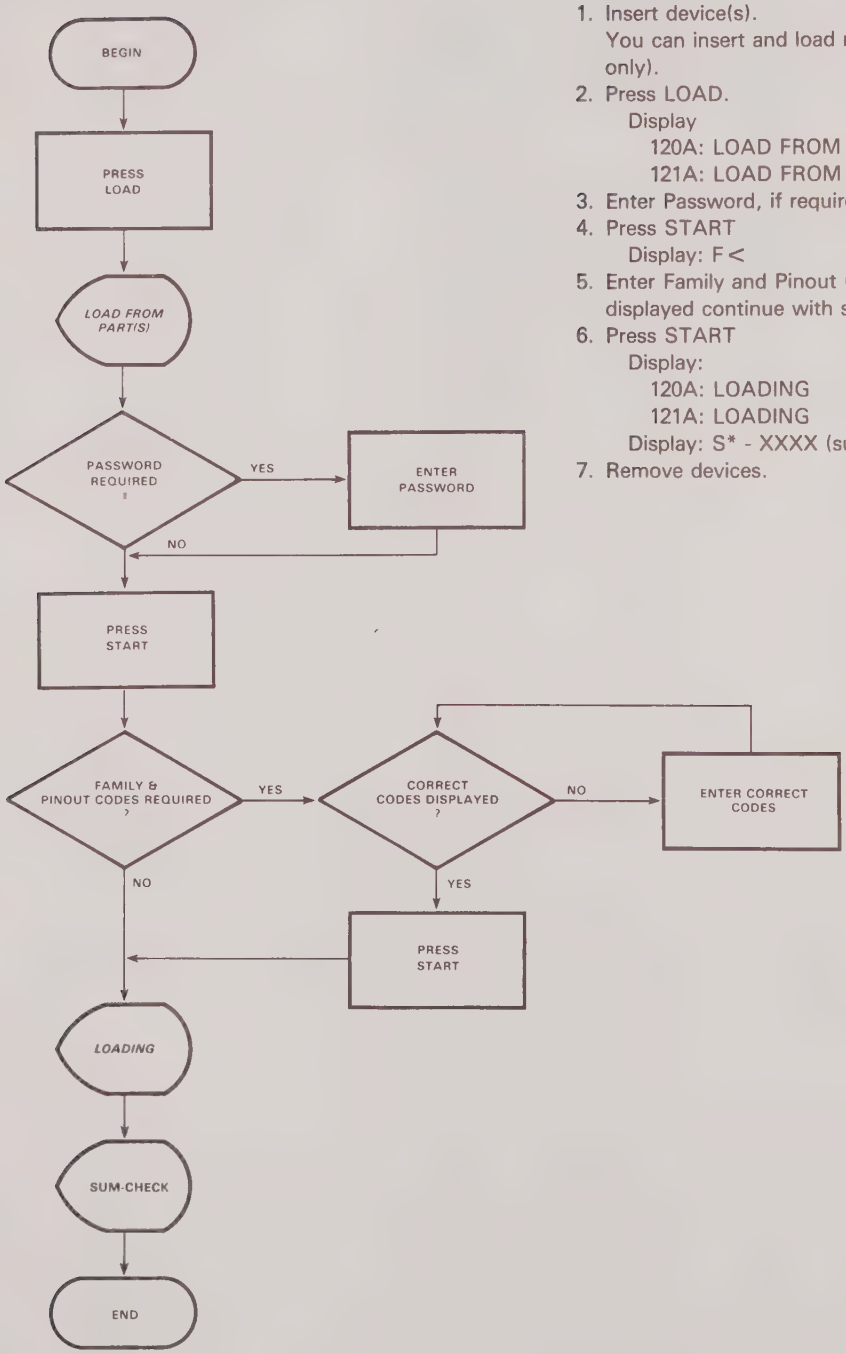


Figure 3-6. Load From Parts

Use this procedure to load RAM from a DCU or other data source. Make sure that the peripheral is ready to send data and, if necessary, the correct I/O Offset in place on the programmer.

1. Press LOAD
   Display
   120A/Peripheral or DCU: LOAD FROM PART
   121A/Peripheral or DCU: LOAD FROM PARTS
2. Press LOAD
   Display
   120A or 121A with Peripheral: LOAD FROM PORT
   120A or 121A with DCU: LOAD FROM FILE
3. Enter Password if required. If not, continue to step 4.
4. Press START
   Display
   120A or 121A with Peripheral: FORMAT-XXXV
   120A or 121A with DCU: PN - <
5. Enter
   120A or 121A with Peripheral: data translation format code.
   120A or 121A with DCU: part number (name of the file).
6. Press START
   Display
   120A or 121A with Peripheral: LOADING PORT
   120A or 121A with DCU: LOADING FILE
   Display
   120A or 121A with Peripheral: S* - XXXX (sum-check)
   120A or 121A with DCU: PN - < (name of the file)

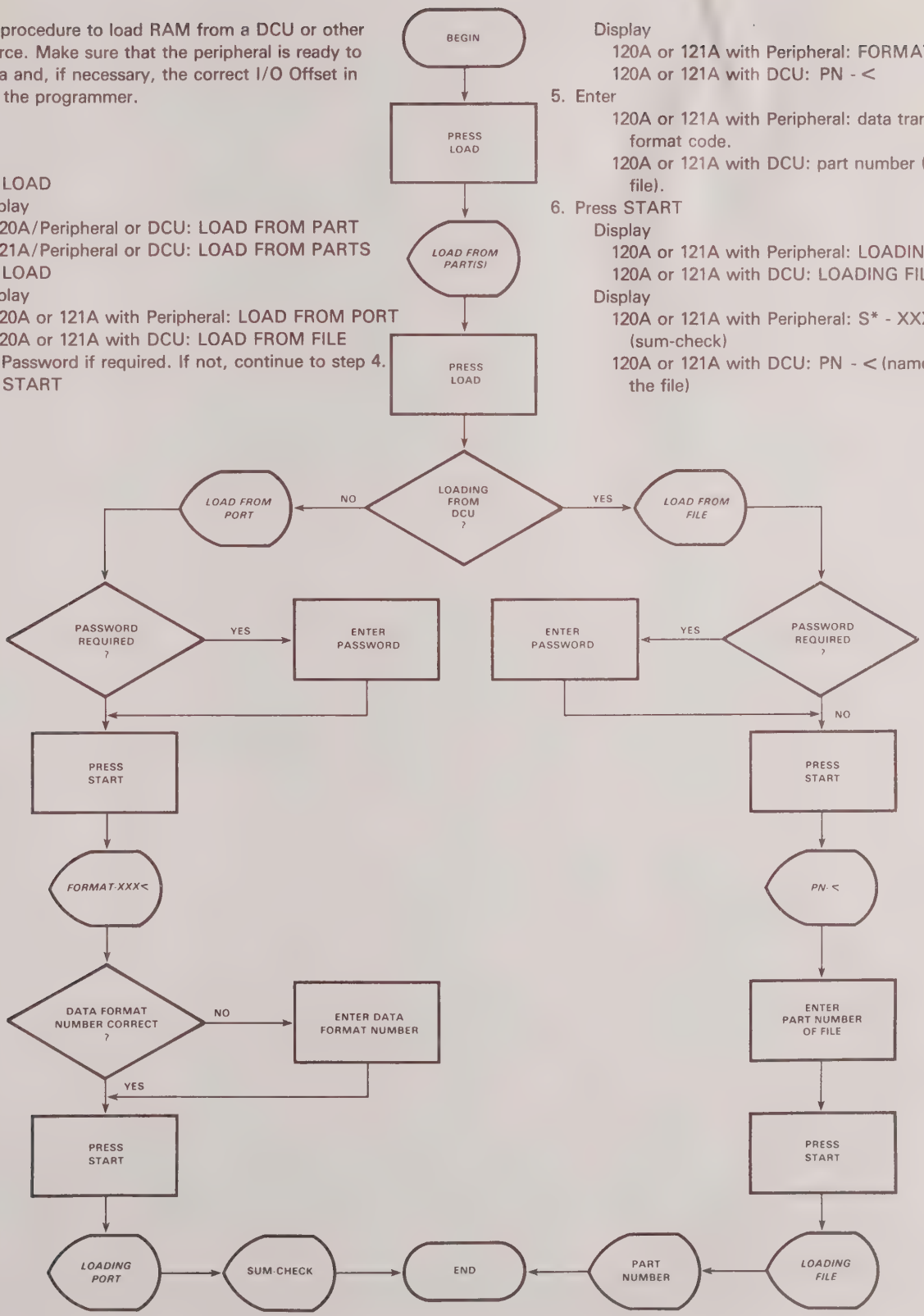
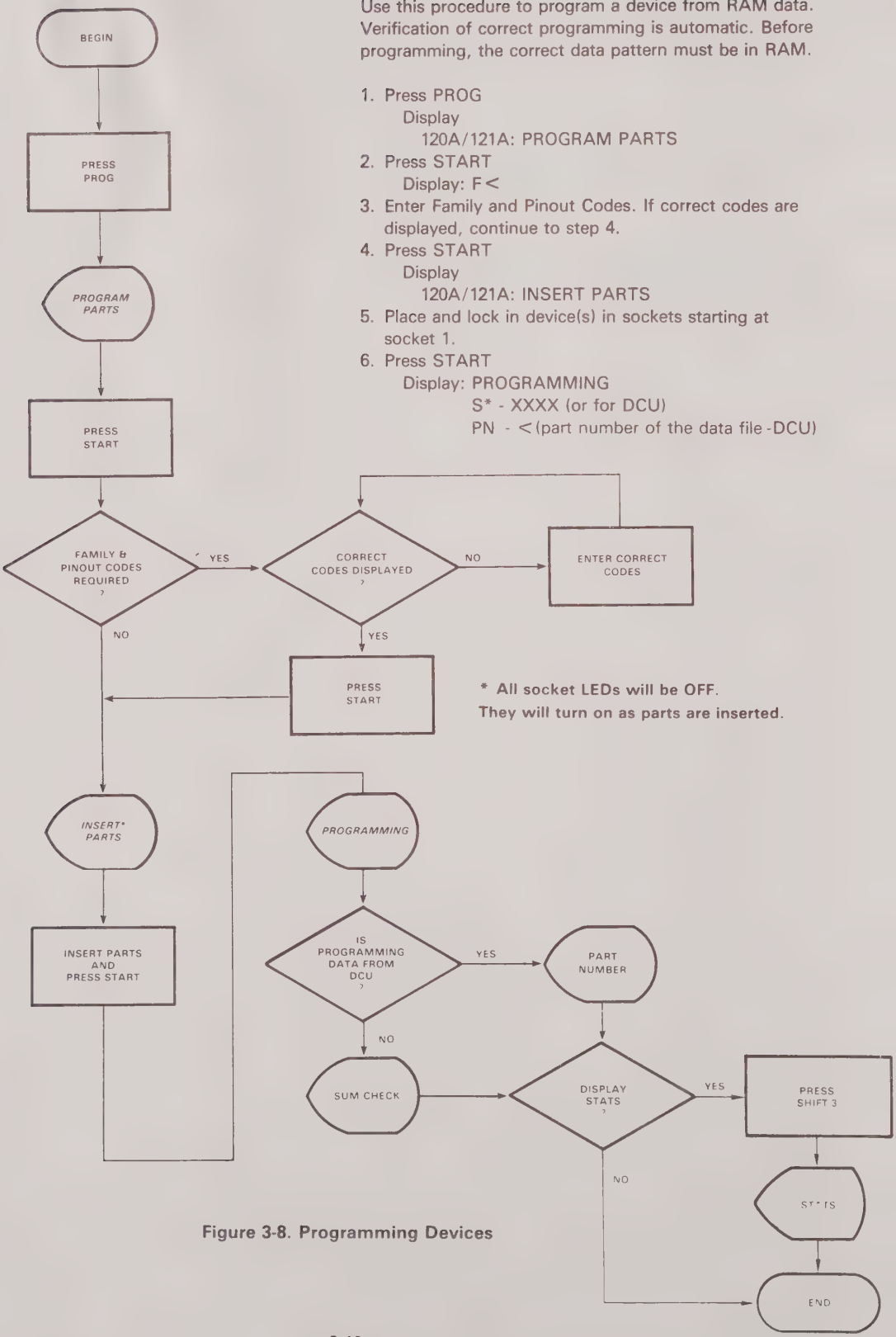


Figure 3-7. Load From Port/File

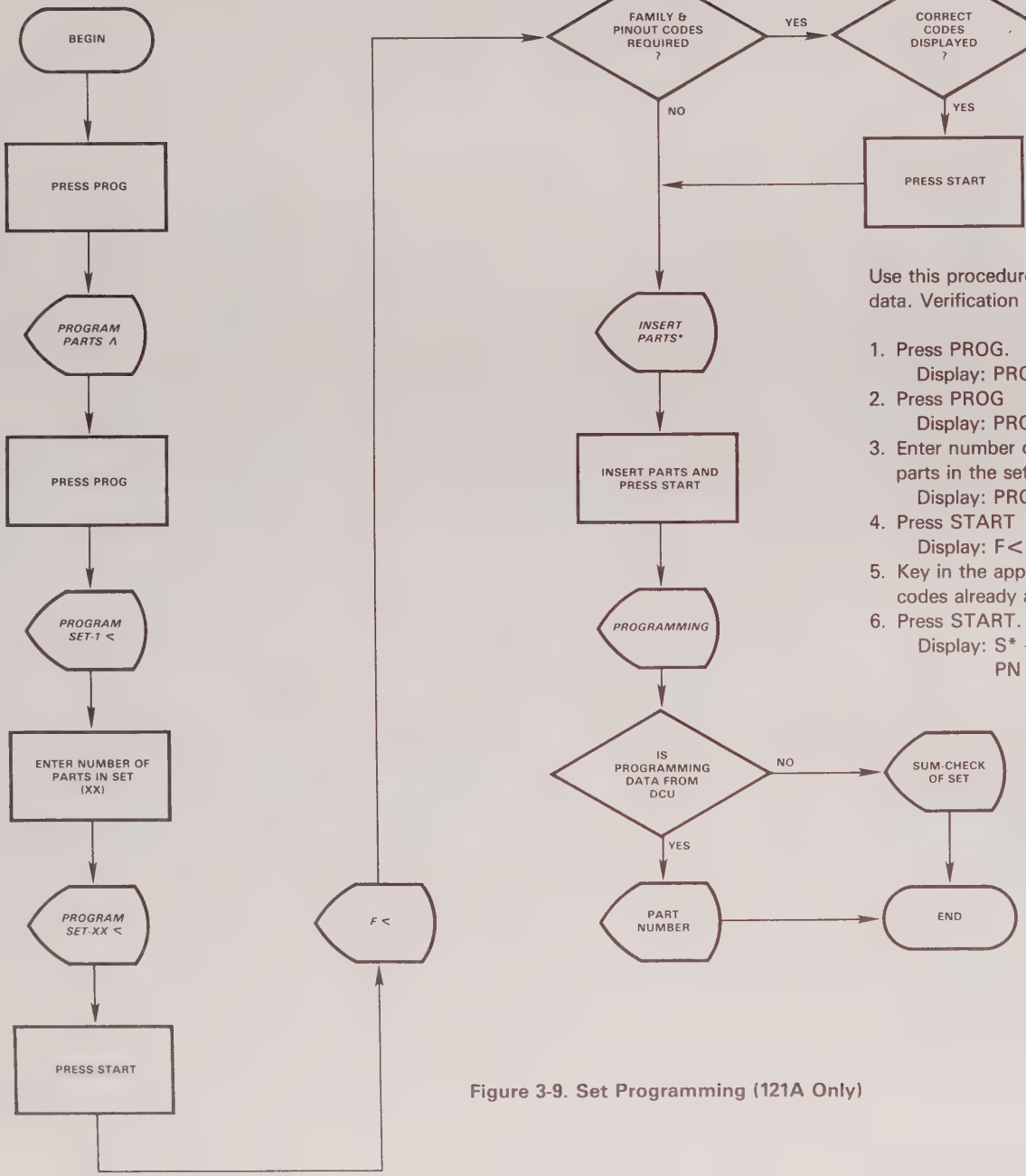
Use this procedure to program a device from RAM data. Verification of correct programming is automatic. Before programming, the correct data pattern must be in RAM.

1. Press PROG
   Display
   120A/121A: PROGRAM PARTS
2. Press START
   Display: F<
3. Enter Family and Pinout Codes. If correct codes are displayed, continue to step 4.
4. Press START
   Display
   120A/121A: INSERT PARTS
5. Place and lock in device(s) in sockets starting at socket 1.
6. Press START
   Display: PROGRAMMING
   S* - XXXX (or for DCU)
   PN - <(part number of the data file -DCU)



* All socket LEDs will be OFF. They will turn on as parts are inserted.

Figure 3-8. Programming Devices

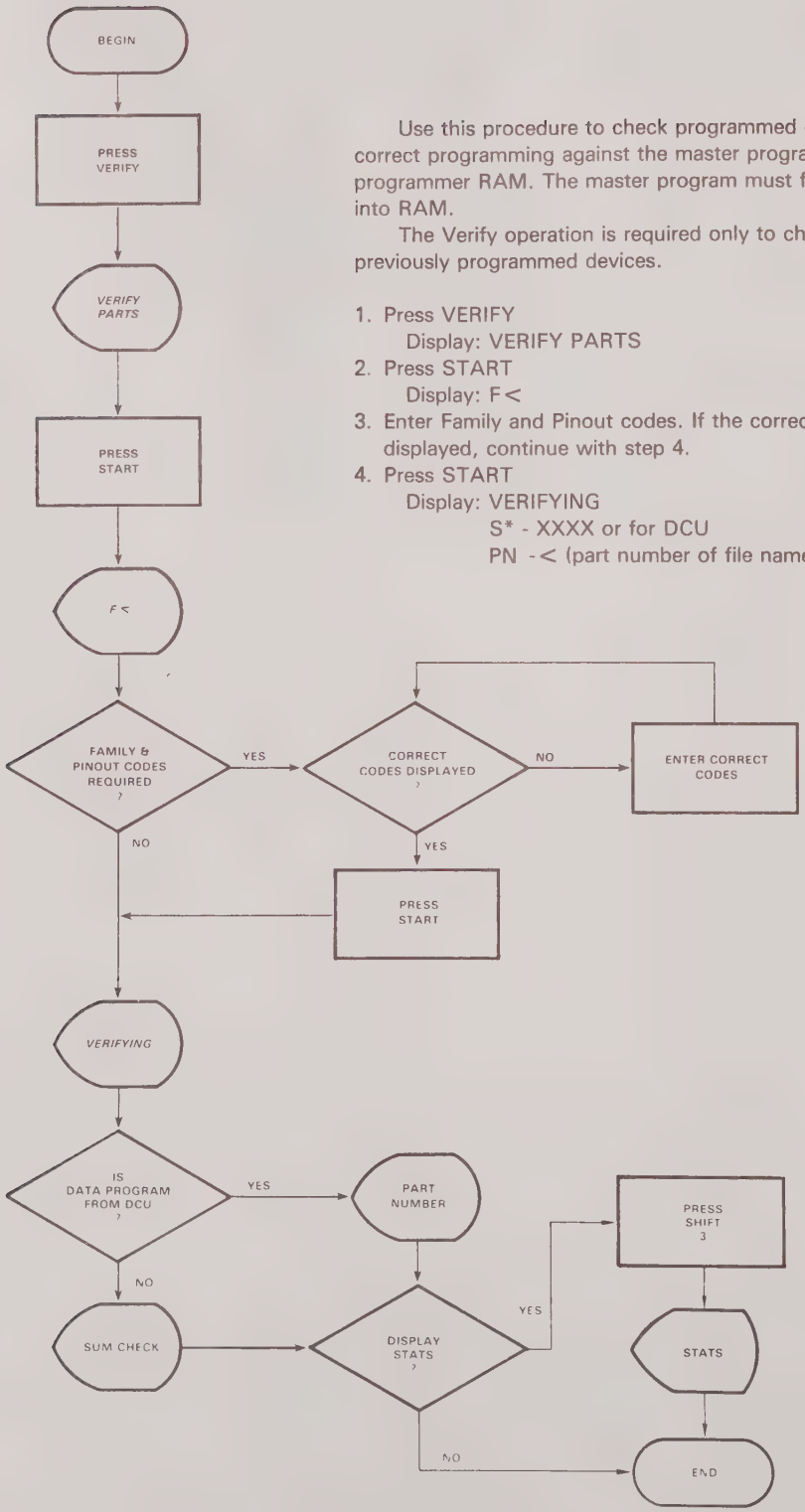


Use this procedure to program a set of devices from RAM data. Verification of correct programming is automatic.

1. Press PROG.
   Display: PROGRAM PARTS
2. Press PROG
   Display: PROGRAM SET - 1<
3. Enter number of parts in set. If the correct number of parts in the set is displayed, continue with step 4.
   Display: PROGRAM SET - XX<
4. Press START
   Display: F<
5. Key in the appropriate Family and Pinout Codes. If these codes already appear, continue with step 6.
6. Press START. Display: PROGRAMMING
   Display: S* - XXXX, or for DCU
   PN - < (part number of data file)

*** All socket LEDs will be OFF. They will turn on as parts are inserted.**

Figure 3-9. Set Programming (121A Only)

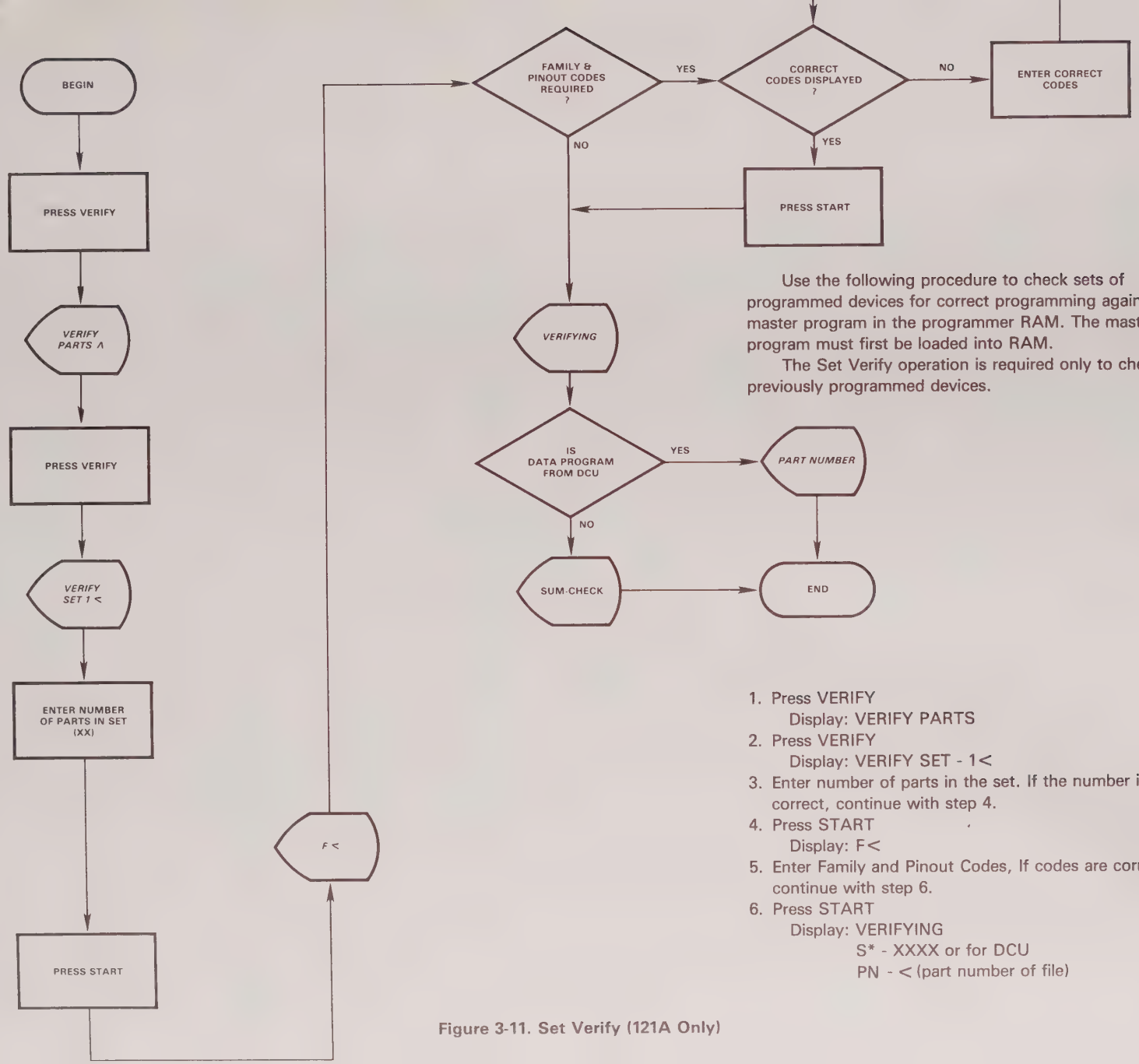


Use this procedure to check programmed devices for correct programming against the master program in the programmer RAM. The master program must first be loaded into RAM.

The Verify operation is required only to check previously programmed devices.

1. Press VERIFY
   Display: VERIFY PARTS
2. Press START
   Display: F<
3. Enter Family and Pinout codes. If the correct codes are displayed, continue with step 4.
4. Press START
   Display: VERIFYING
   S* - XXXX or for DCU
   PN -< (part number of file name)

Figure 3-10. Verifying Programmed Devices

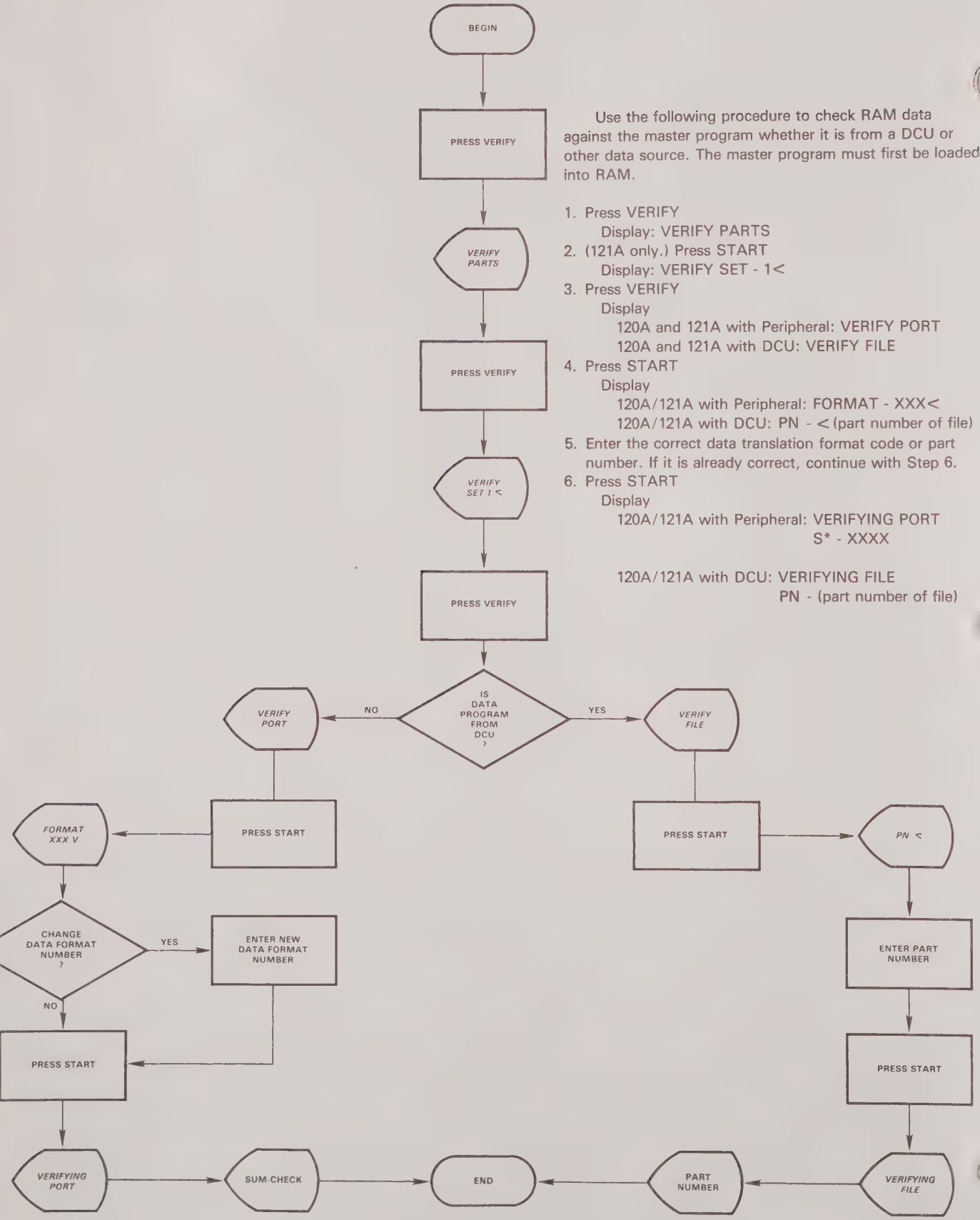


Use the following procedure to check sets of programmed devices for correct programming against the master program in the programmer RAM. The master program must first be loaded into RAM.

The Set Verify operation is required only to check previously programmed devices.

1. Press VERIFY
   Display: VERIFY PARTS
2. Press VERIFY
   Display: VERIFY SET - 1<
3. Enter number of parts in the set. If the number is already correct, continue with step 4.
4. Press START
   Display: F<
5. Enter Family and Pinout Codes, If codes are correct, continue with step 6.
6. Press START
   Display: VERIFYING
   S* - XXXX or for DCU
   PN - < (part number of file)

Figure 3-11. Set Verify (121A Only)



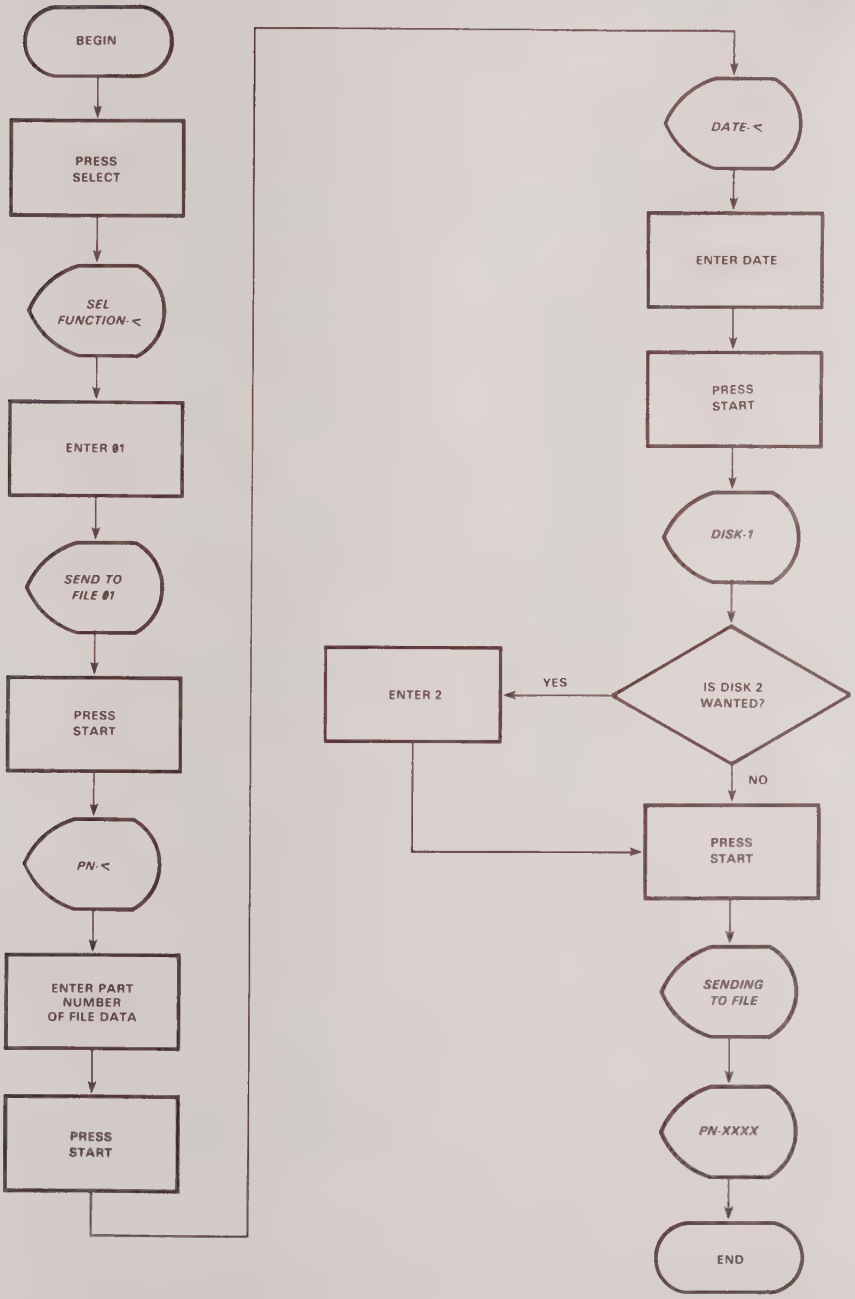
Use the following procedure to check RAM data against the master program whether it is from a DCU or other data source. The master program must first be loaded into RAM.

1. Press VERIFY
   Display: VERIFY PARTS
2. (121A only.) Press START
   Display: VERIFY SET - 1<
3. Press VERIFY
   Display
   120A and 121A with Peripheral: VERIFY PORT
   120A and 121A with DCU: VERIFY FILE
4. Press START
   Display
   120A/121A with Peripheral: FORMAT - XXX<
   120A/121A with DCU: PN - < (part number of file)
5. Enter the correct data translation format code or part number. If it is already correct, continue with Step 6.
6. Press START
   Display
   120A/121A with Peripheral: VERIFYING PORT
   S* - XXXX

   120A/121A with DCU: VERIFYING FILE
   PN - (part number of file)

Figure 3-12. Verifying RAM From the Serial Port

This Select Function sends data in the programmer RAM to the DCU.



NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

Figure 3-13. Send to File

This Select Function copies a specified file from disk 1 onto disk 2 of the DCU.

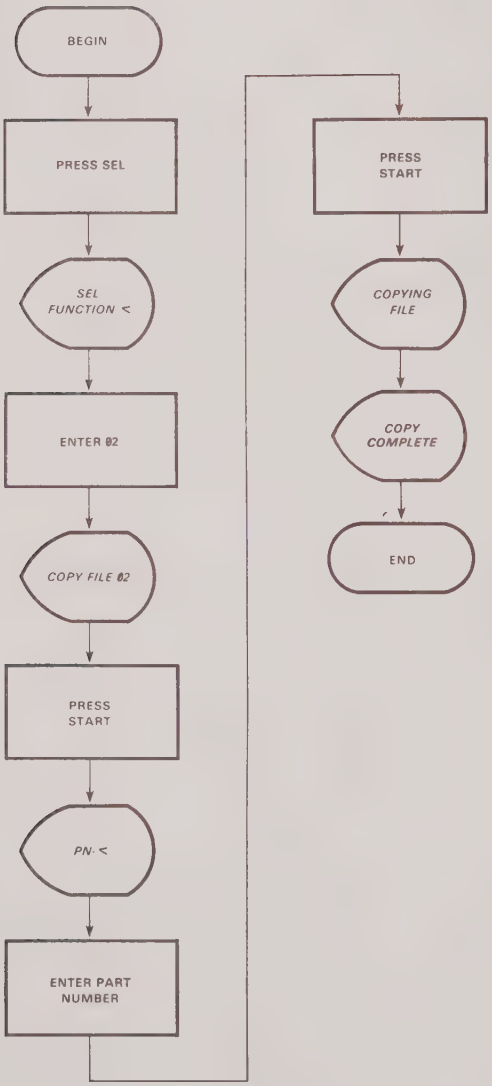


Figure 3-14. Copy File

This Select Function deletes a specifie file from disk 1 on the DCU.

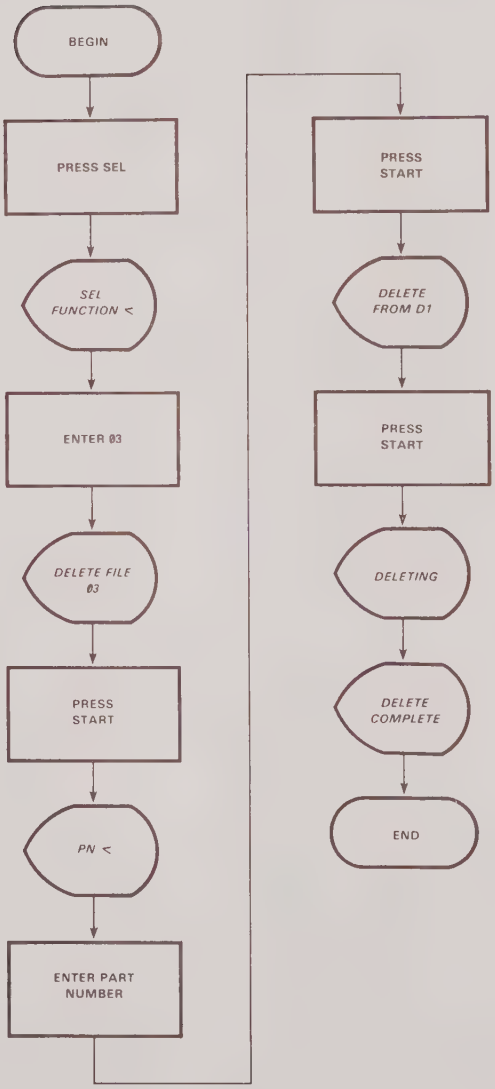


Figure 3-15. Delete File

NOTE
To correct a miscued Select Function, simply press SELECT again and enter the correct code.

This Select Function copies disk 1 of the DCU onto disk 2.

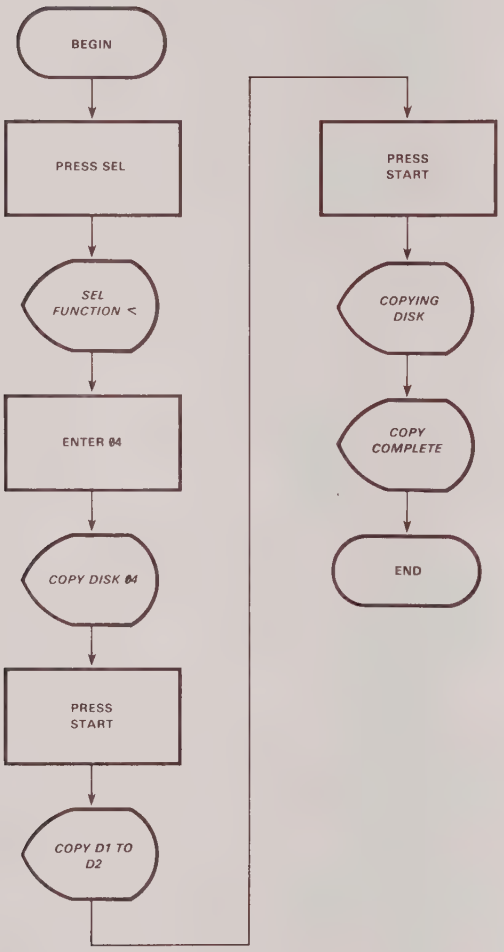


Figure 3-16. Copy Disk

This Select Function formats disk 1 of the DCU. This function takes approximately 5 minutes to execute. Do not attempt any front panel operations during formatting or the function will abort, resulting in an unformatted disk.

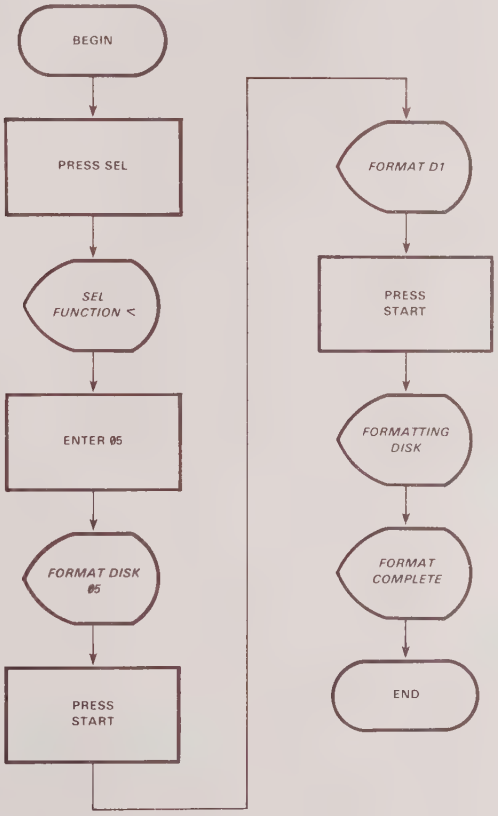


Figure 3-17. Format Disk

NOTE
To correct a miscued Select Function, simply press SELECT again and enter the correct code.

This Select Function lists the file part numbers stored on the disk.

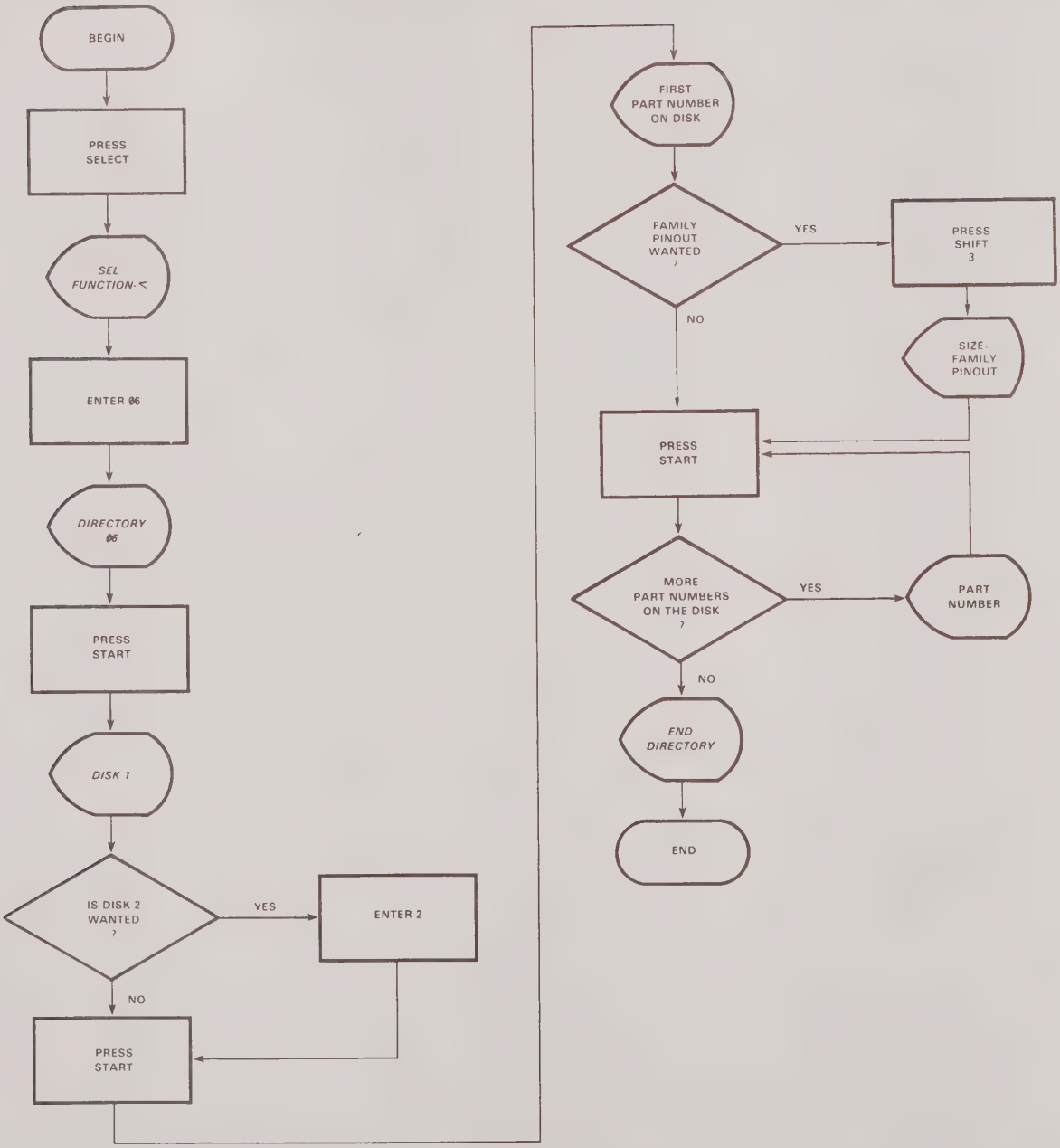
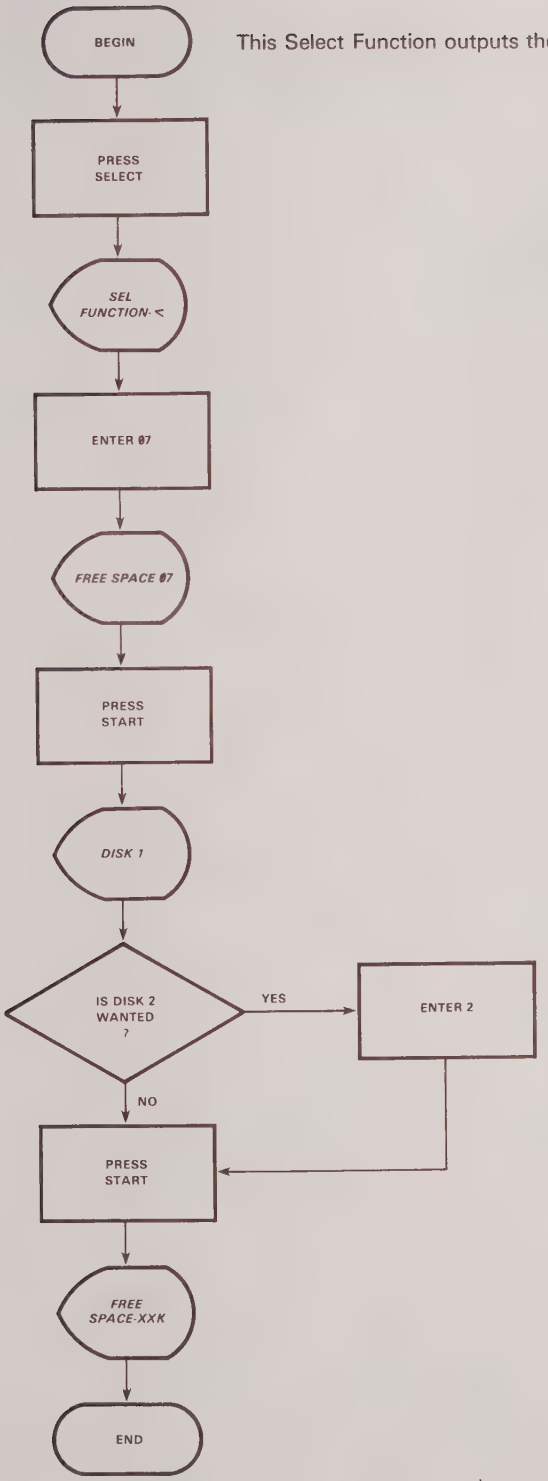


Figure 3-18. Directory

NOTE
To correct a miscued Select Function, simply press SELECT again and enter the correct code.



This Select Function outputs the free space available on the disk.

Figure 3-19. Free Space

NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

This Select Function sends data in RAM to the serial port.

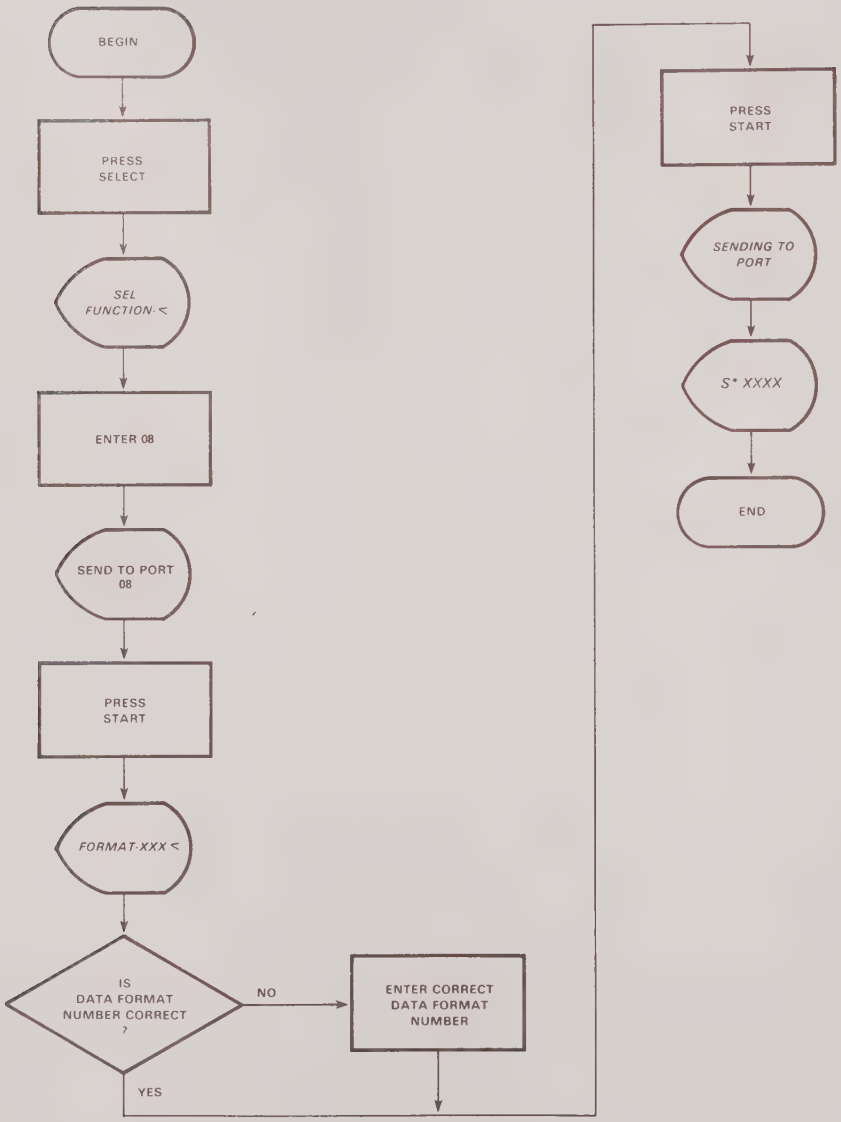


Figure 3-20. Send to Port

NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

This Select Function puts the programmer under remote control.

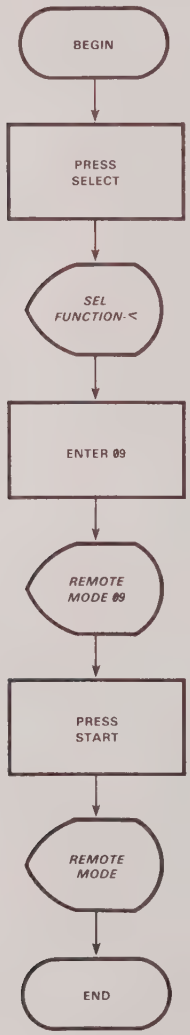


Figure 3-21. Remote Mode

This Select Function outputs the software configuration number, which identifies the revision level of your software in the programmer. It also displays your programmer RAM size and software version number. This Select Function is not required in normal, everyday operations.

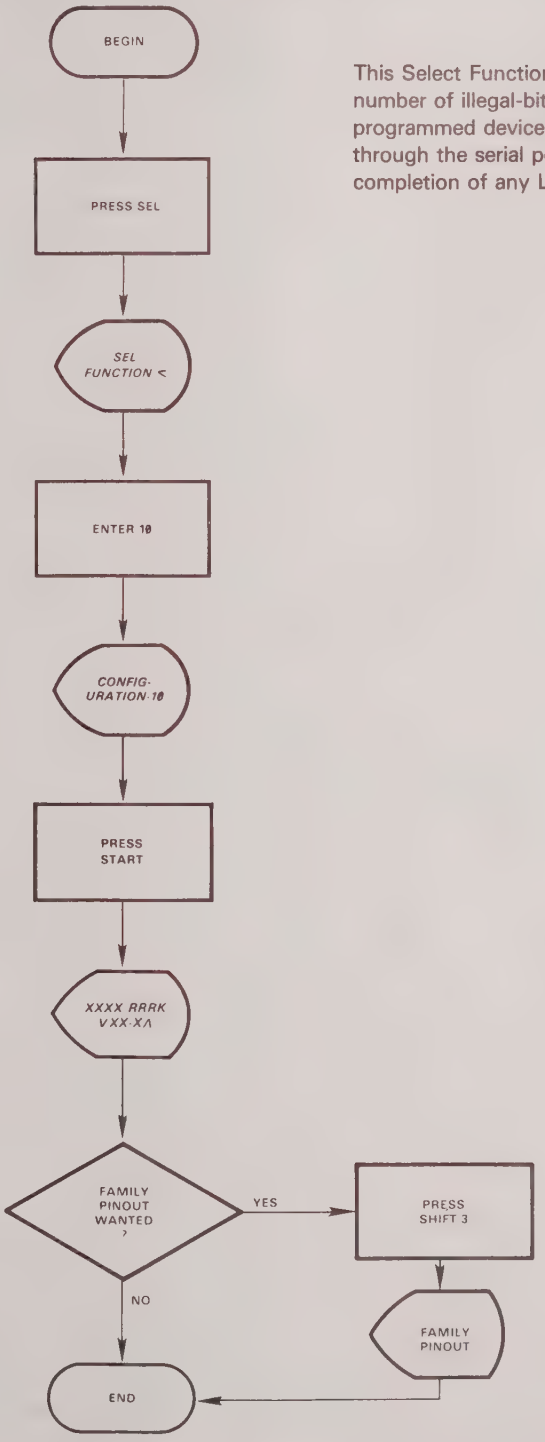


Figure 3-22. Configuration Number

This Select Function allows the operator to transmit the number of illegal-bit errors, number of successfully programmed devices, and the number of verification errors through the serial port. These numbers will be cleared upon completion of any LOAD operation.

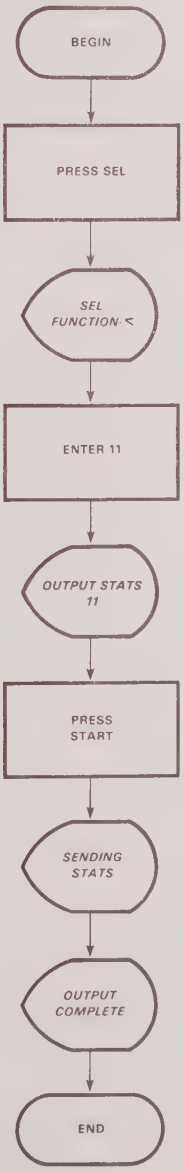
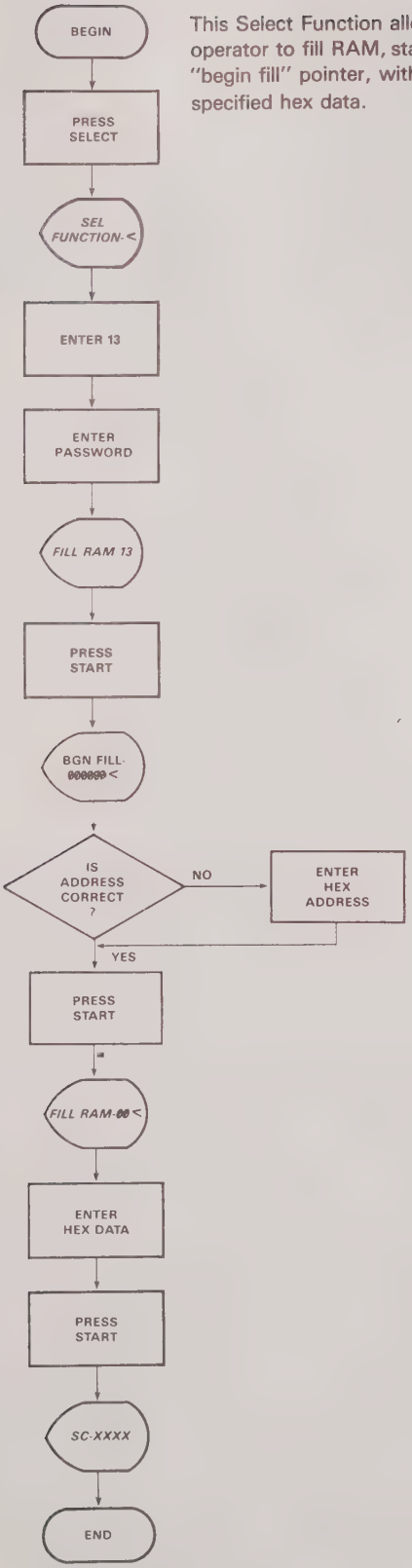


Figure 3-23. Output Statistics

NOTE

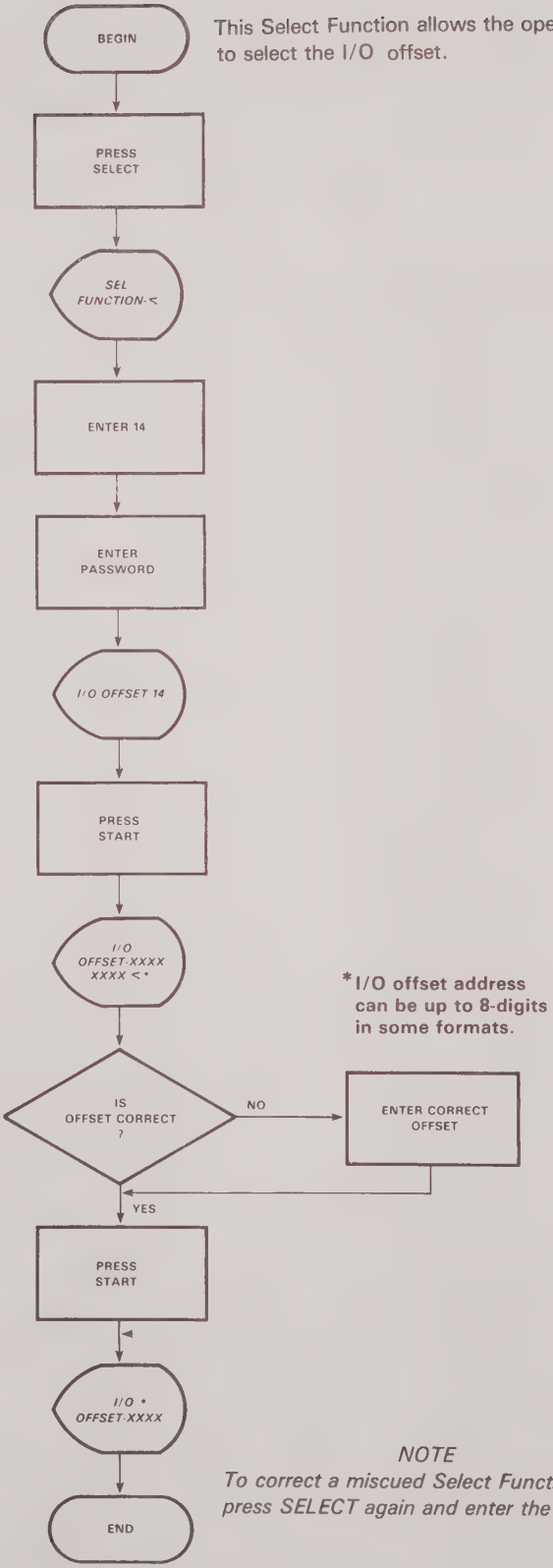
To correct a miscued Select Function, simply press SELECT again and enter the correct code.

**NOTE: Family and Pinout Code in effect can be displayed by Pressing SHIFT 3.*



This Select Function allows the operator to fill RAM, starting at the "begin fill" pointer, with the specified hex data.

Figure 3-24. Fill RAM
Only with Data Lock off.



This Select Function allows the operator to select the I/O offset.

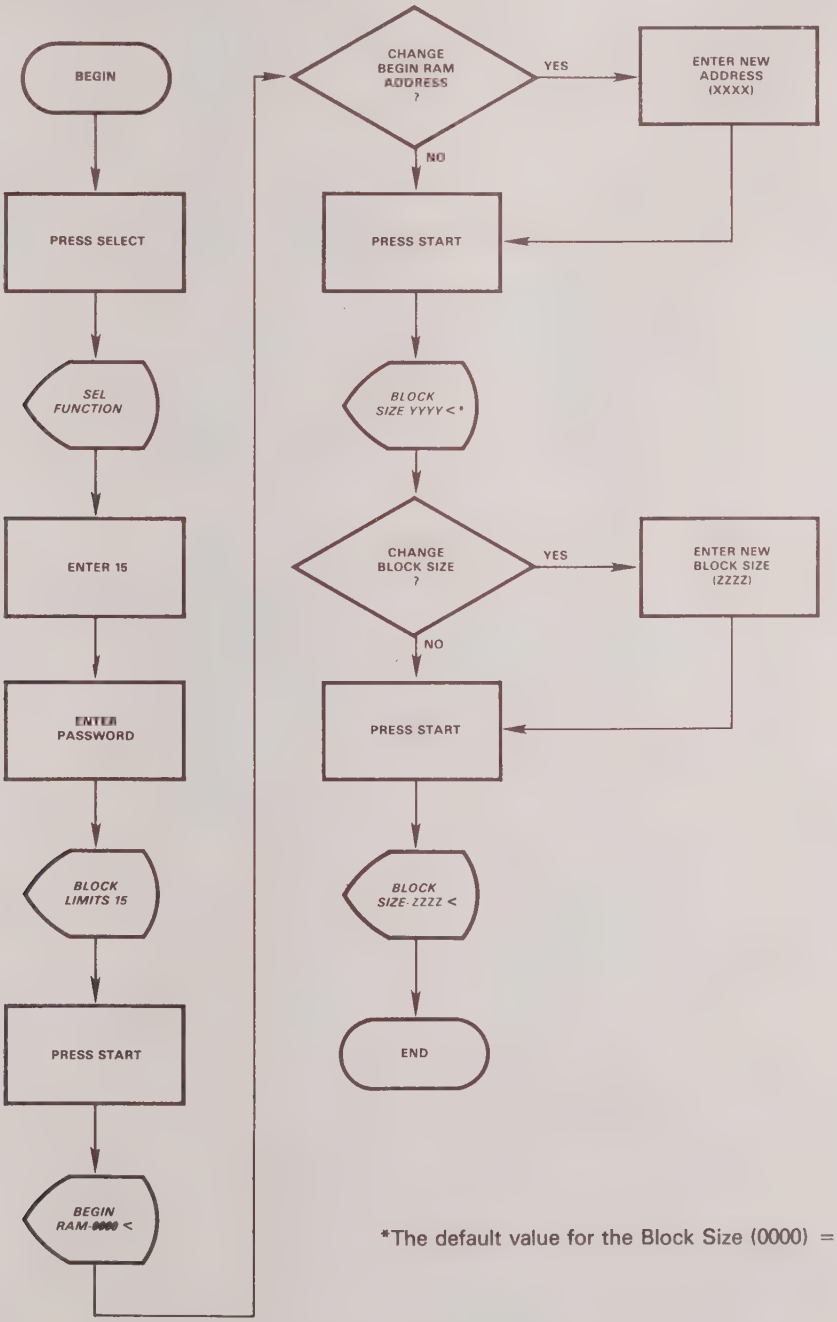
***I/O offset address can be up to 8-digits in some formats.**

NOTE
To correct a miscued Select Function, simply press SELECT again and enter the correct code.

Figure 3-25. I/O Offset.
Only with Data Lock off.

This select function sets the first RAM address from which data will move and the number of bytes that will be moved in an I/O or device operation. With the block size set less than or equal to the word limit of the device, the number of bytes moved will be equal to the block size times the number of devices in the set. The number of bytes moved will be equal to the block size, if the block size is greater than the device size.

The default for the first address, and the number of bytes moved, are, respectively, zero and the device size times the set size. A zero block size will cause a devault to the device word limit times the set size.



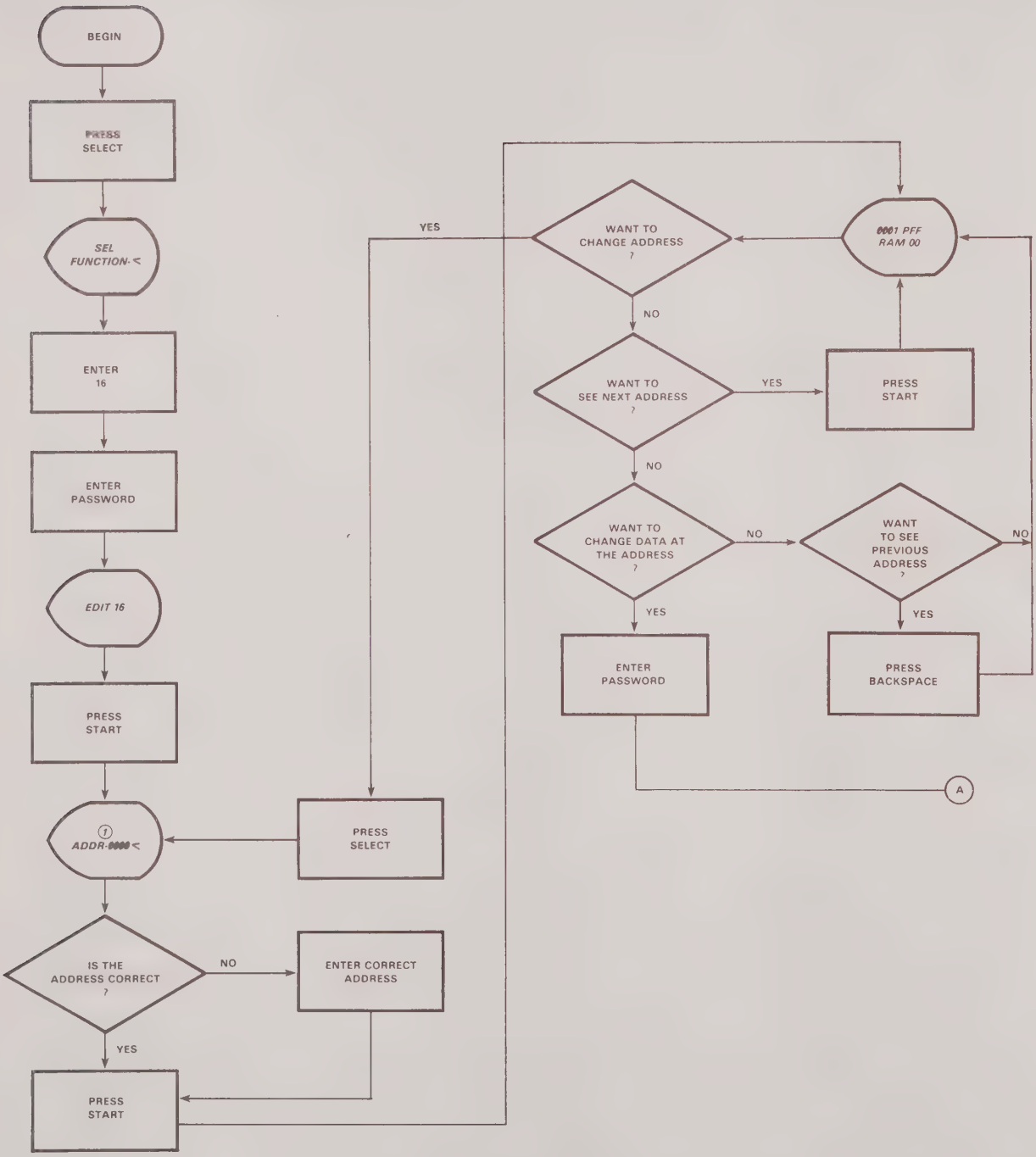
*The default value for the Block Size (0000) = device size.

Figure 3-26. Block Limits
Only with Data Lock off

NOTE
To correct a miscued Select Function, simply press SELECT again and enter the correct code.

NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.



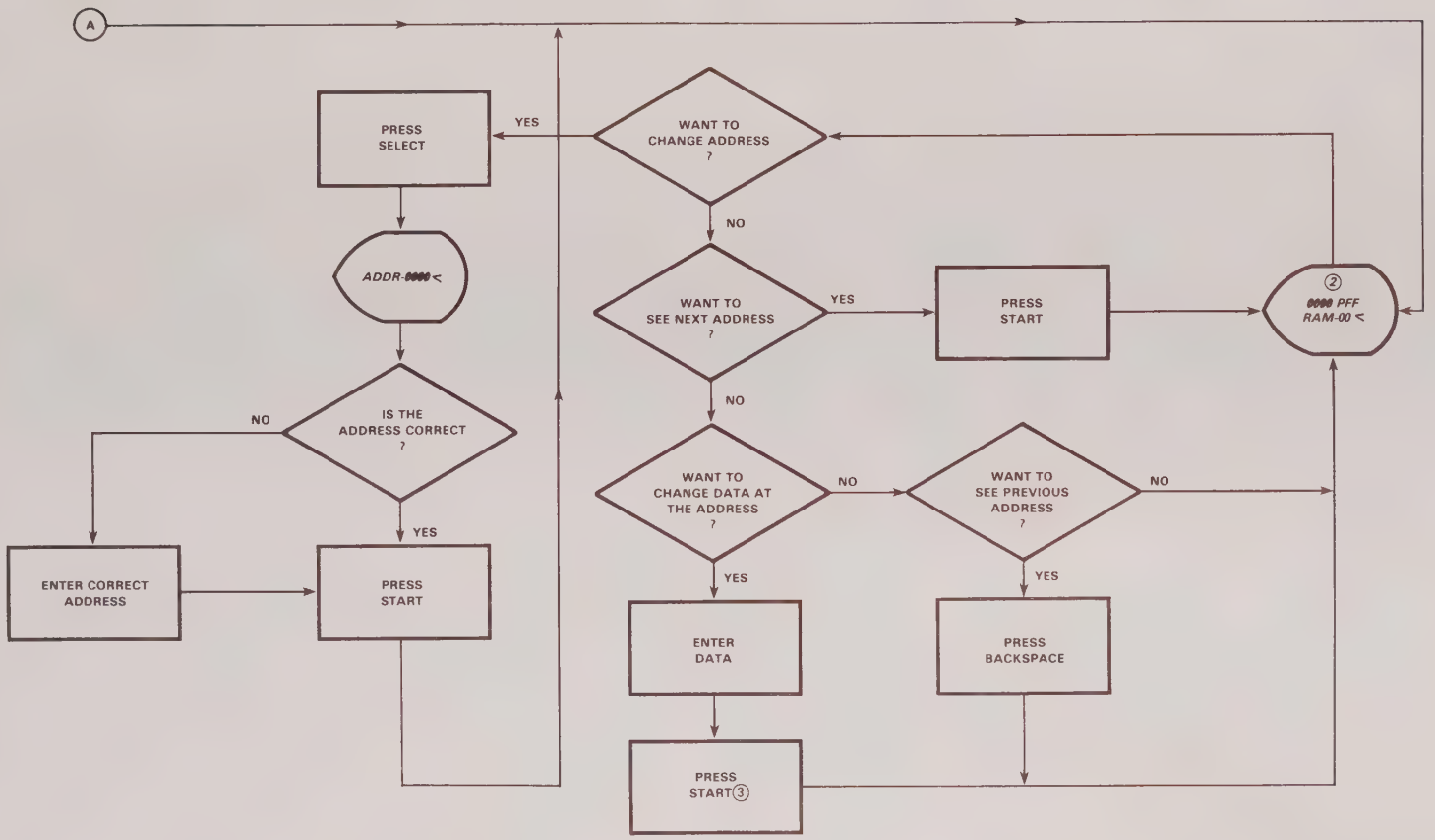
Only with Data Lock off.

This Select Function allows the operator to edit RAM data.

Figure 3-27. Edit

NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

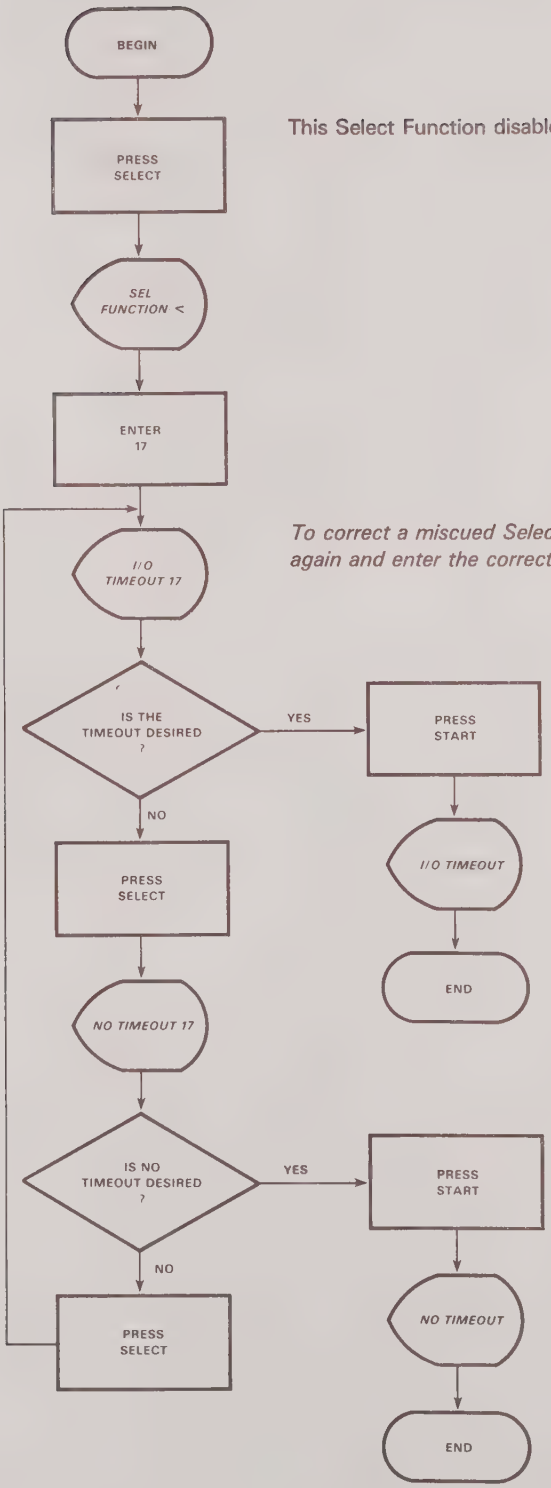


NOTES

1. 000000 PFF R-00
   - 000000 — Address
   - PFF — Data in Device
   - R-00 — Data in RAM

2. *The < character means the value may be changed.*
3. *The data entered will be stored and the address incremented.*
4. *To exit the Edit mode at any point in the procedure, press PROG, VERIFY, or LOAD.*

Figure 3-27. Edit (Continued)



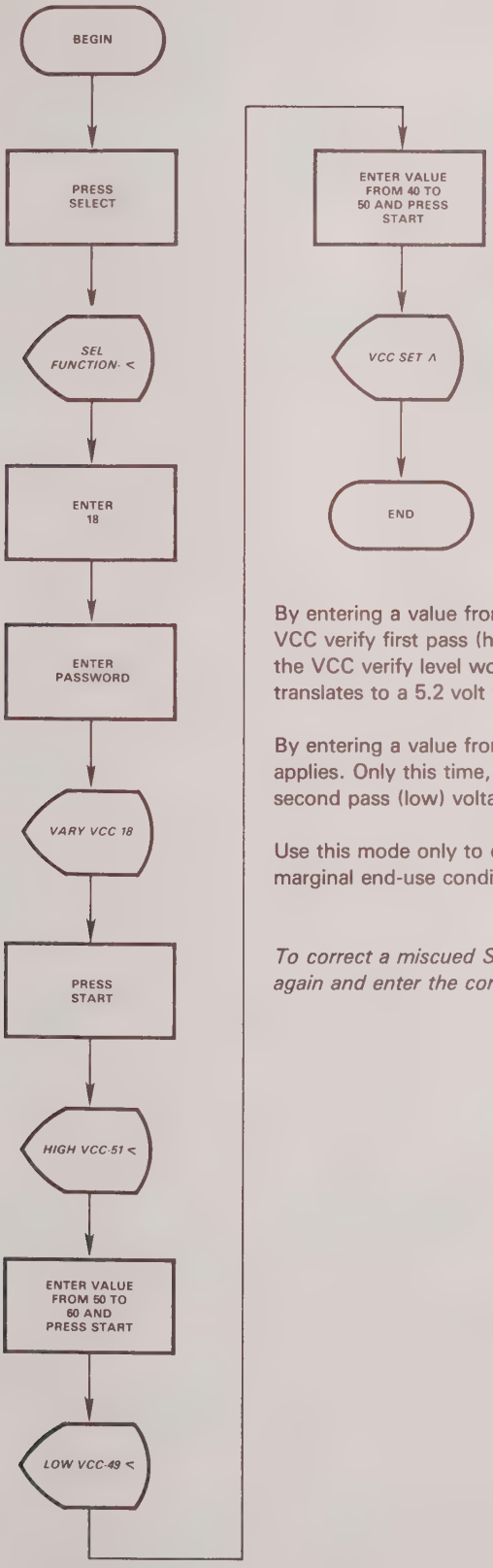
This Select Function disables the programmer's I/O timeout.

NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

Figure 3-28. Timeout Disable

This Select Function allows the operator to vary the VCC Verify levels.



By entering a value from 50 to 60, you are able to vary the VCC verify first pass (high) voltage. If you were to enter 51, the VCC verify level would be 5.1 volts and a value of 52 translates to a 5.2 volt verify, and so on.

By entering a value from 40 to 50, the same procedure applies. Only this time, the value corresponds to VCC verify second pass (low) voltage.

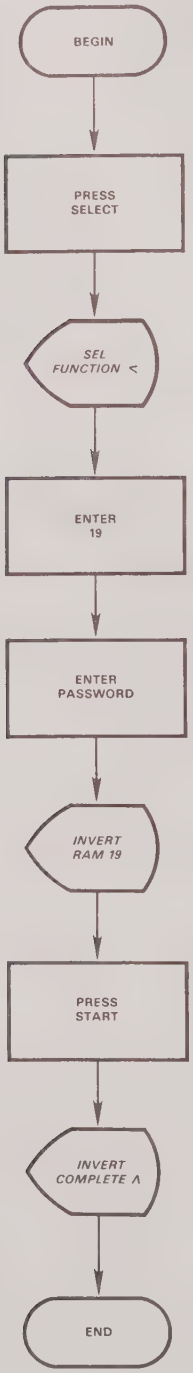
Use this mode only to check for performance under marginal end-use conditions.

NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

Figure 3-29. Vary VCC

This Select Function allows the operator to invert the data in the programmer RAM.

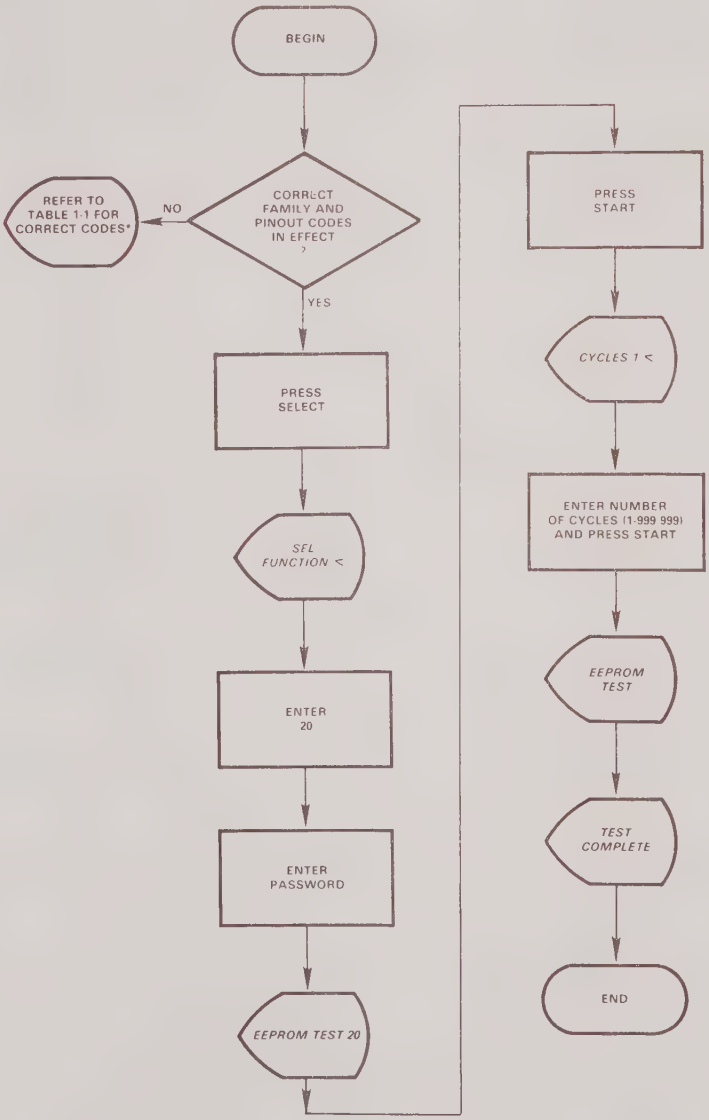


NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

Figure 3-30. Invert Ram

This test determines whether or not your EEPROM is programmable. It accomplishes this by programming and erasing the EEPROM once in each cycle. Each cycle takes approximately 30 seconds. Enter only the number of cycles necessary for testing.



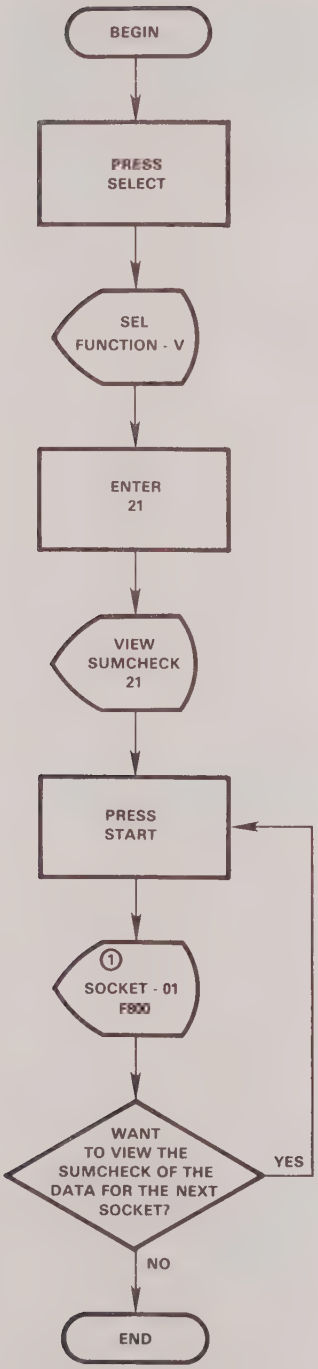
***Now, enter the correct codes in a program operation sequence (see section 3).**

This Select Function allows the operator to functionally test EEPROM devices.

NOTE

To correct a miscued Select Function, simply press SELECT again and enter the correct code.

Figure 3-31. EEPROM Test



This Select Function shows the sum-check of the RAM data destined for each socket; depending on the set size and the device selected.

1. SOCKET - 01
   The number of the socket whose corresponding RAM data is being summed

F800
The sum-check of the RAM data for the indicated socket

Figure 3-32. View Sum-Check

This mode allows the operator to convert the 121A into a 16-bit programmer. When this mode is in efect, the programmer will perform device-related operations (Load, Program and Verify) as if each pair of 8-bit-wide PROMs were a single 16-bit-wide device. This mode can be used either from the front panel or in remote control.

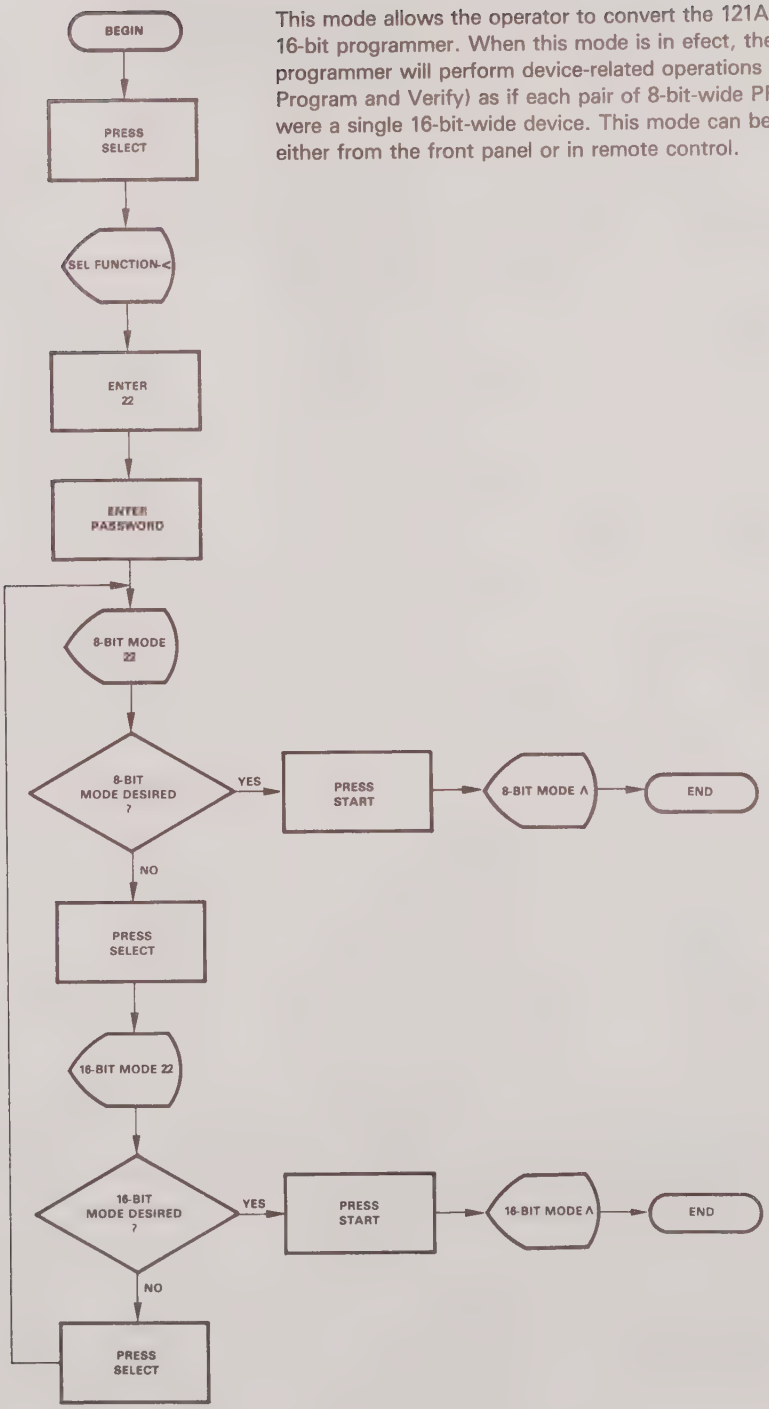


Figure 3-33. 16-Bit Mode

This Select Function allows the user to select either a quicker single-pass verify at nominal voltages of the parametric two-pass verify normally in effect.

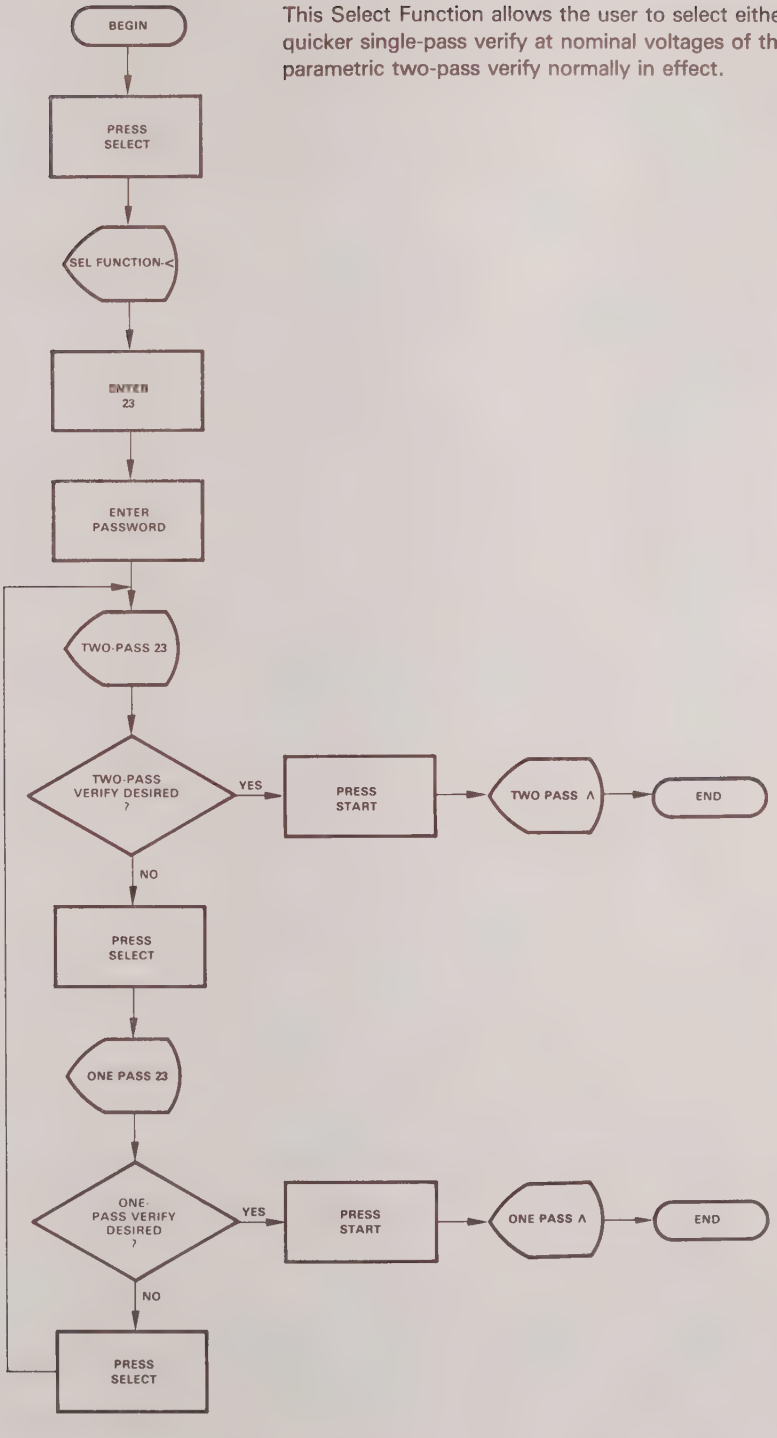


Figure 3-34. One- or Two-Pass Verify

This Select Function allows the operator to view the electronic ID of the device installed in the lowest numbered socket.

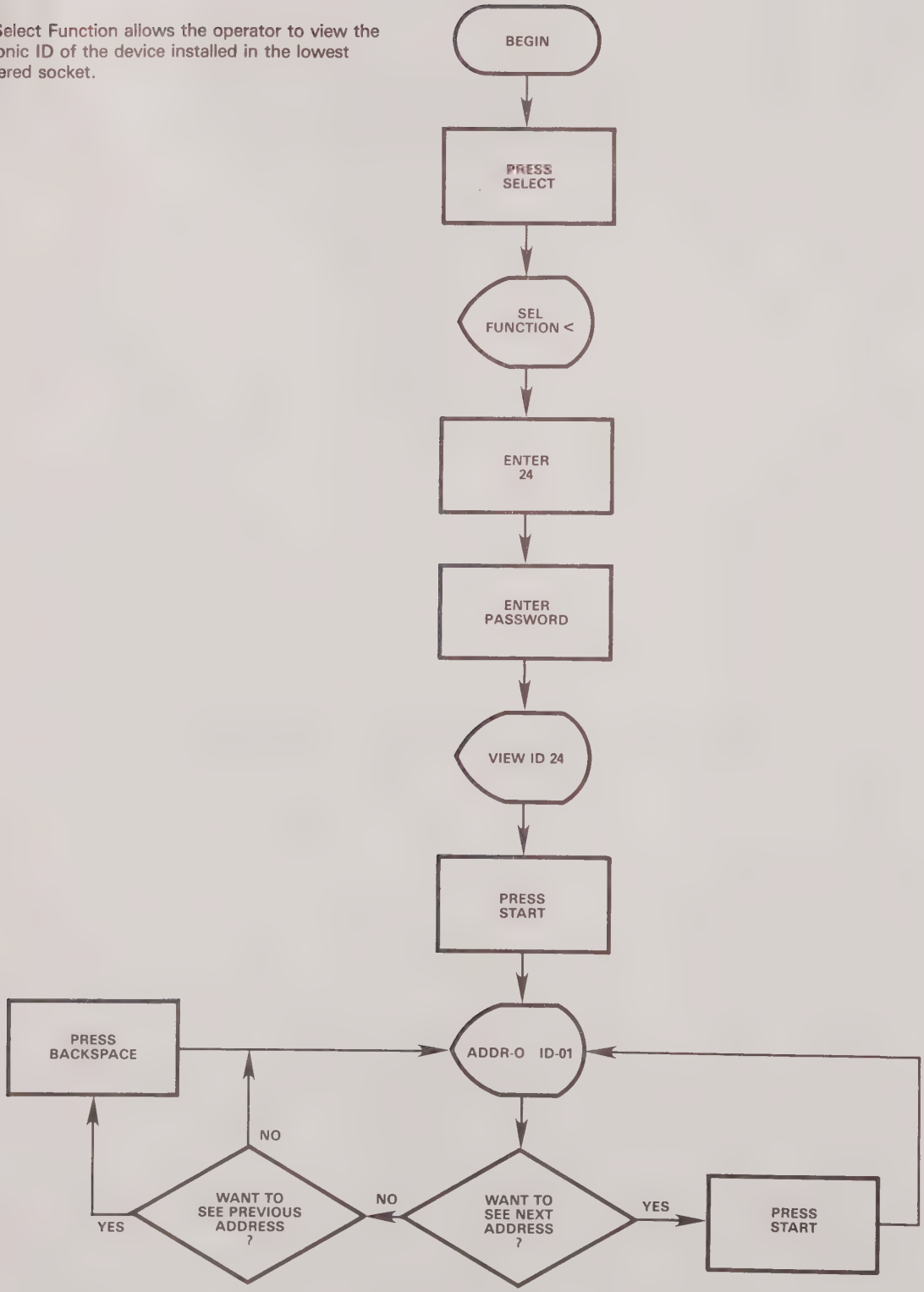


Figure 3-35. View Electronic Identification

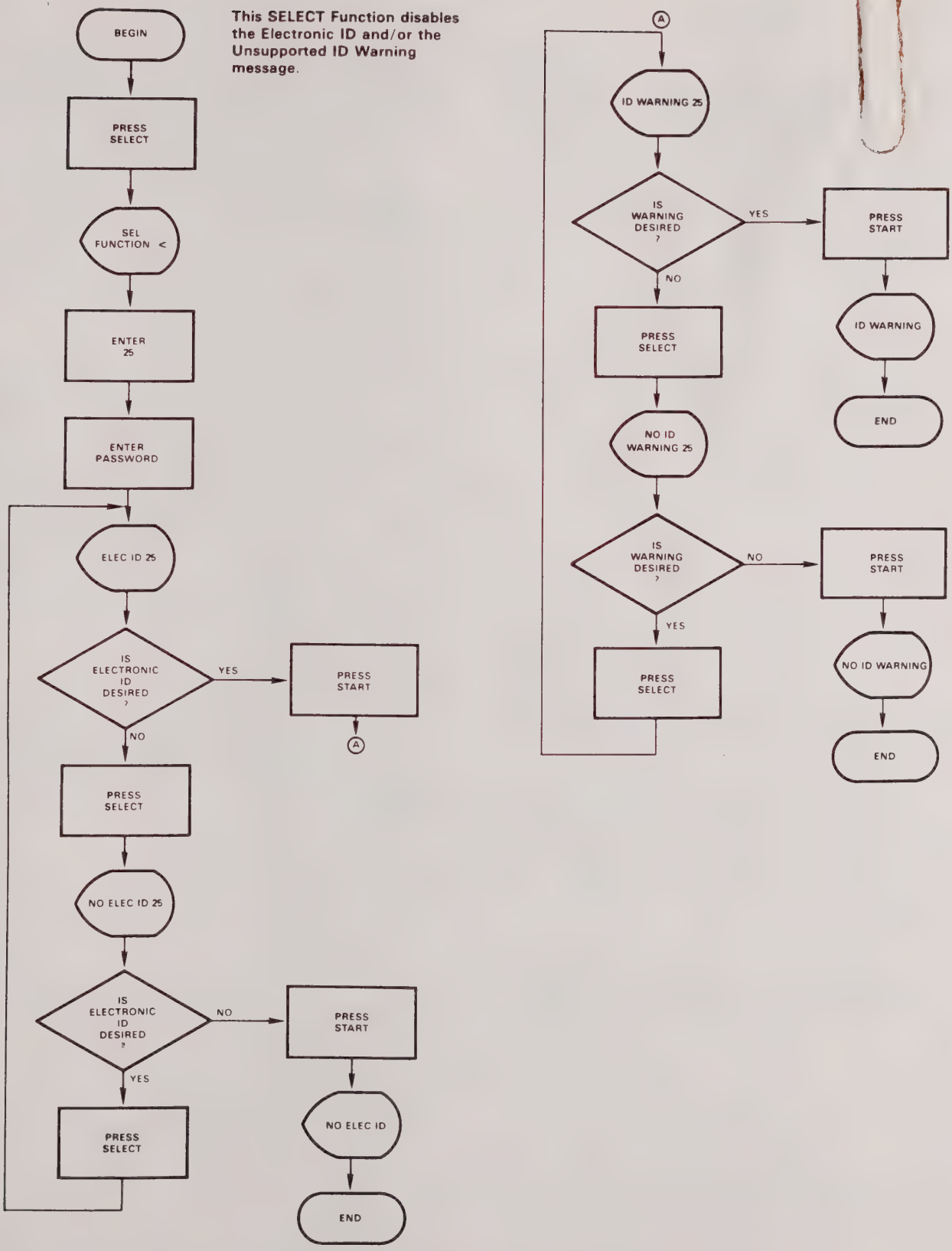


Figure 3-36. Electronic ID Options

3.6 REMOTE CONTROL

This section describes the command set available for data transfer, programming and verification by remote control. Remote control commands can be written into a computer's operating software, allowing the computer or terminal to control the programmer as it would any peripheral device. Commands are generated by the computer software or in response to entries from a terminal and are sent to the programmer, which executes the command (or tries to) and sends the appropriate response to the controlling instrument.

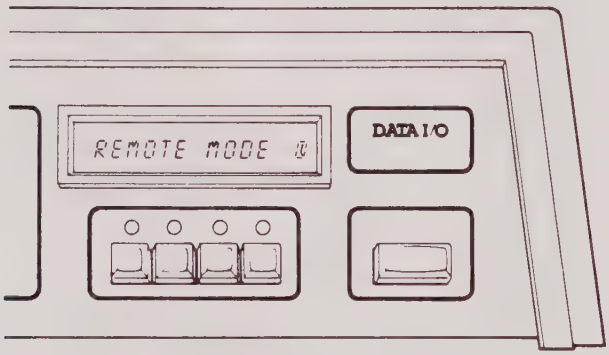


Figure 3-37. Remote Control Display

3.6.1 ENTERING AND EXITING REMOTE CONTROL

Before entering remote control, check the parity, stop bits, and baud rate. They must be the same on the programmer and the controlling instrument. These are explained in section 2 of this manual.

- To manually enter remote control: press SELECT, enter 09 and press START. While in remote control, the display will look like Figure 3-37.
- To automatically enter remote control when the programmer is powered up, set switch segment 2 of U4 on the Specific I/O card (701-1835) to ON (see Figure 2-6).
- To Exit:
  1. From a computer or terminal keyboard, enter Z RETURN.
  2. From the programmer keyboard press any of the 4 mode keys (LOAD, PROG, VERIFY, or SELECT).

3.6.2 RESPONSE CHARACTERS

The programmer sends a response character to the computer after receiving any control commands. Table 3-4 shows how to interpret each response character.

Table 3-4. Response Characters

The programmer sends this response character to the computer	In these cases.
>CRLF*	1. On entering remote control. 2. After successfully executing a command. 3. After the BREAK or ESC key has halted a command.
F CRLF*	After failing to execute a valid command.
? CRLF*	After receiving an invalid command or message it did not understand

*Carriage return (CR) and line feed (LF) are nonprinting characters. Line feeds are normally disabled unless the "U" command is used.

3.6.3 COMMAND SUMMARY

The remote control commands are listed in Table 3-5. These commands are divided into groups according to the purpose of each and described in detail in sections 3.6.4 through 3.6.7.

Table 3-5. Command Summary

COMMAND	DESCRIPTION
Control Commands	
Return	Executes a command.
ESC (Escape)	Aborts a command.
Break	Aborts a binary transfer or command.
Device Commands	
nnT	Tests for illegal bits in a set or sets of nn devices. The default value is one device per set.*
B	Performs blank check on all devices.
FFPP @	Selects family code (FF) and pinout code (PP).
L	Loads a device or set of devices.
nnP	Programs a set of sets of devices. The default value is one device per set.*
nnV	Verifies a set or sets of devices. The default value is one device per set.*
[	Inquires what the family and pinout codes are.
R	Respond with device parameters (word limit, 4 or 8 bit word width, and VOL or VOH device). 1 = VOL, 0 = VOH
&	Instructs the programmer to enter Insert Parts mode.
nnnnnn20]	Performs EEPROM test. The default value is 1 cycle.
CC]	Inquires for the current electronic identifier family codes and pinout codes.
CD]	Inquires for the electronic identifier codes of the installed device(s).
Utility Commands	
G	Displays the software configuration number, which identifies the revision level of software in your programmer.
nnS	Sends the RAM sum-check to the computer, starting with the Begin RAM address up to the word limit, or up to the block size entered by the semicolon (;) command. With nn equal to the socket, the sum-check of a particular device in a set sill be sent.
X	Inquires for programmer errors (the error code of the last 16 errors that occurred.)
Z	Returns control to the programmer.
hhhh <	**Sets the Begin RAM address to hhhh. (121A only)**
hhhh ;	**Sets the Block size to hhhh, overriding the word limit. (121A only)**
hhhh :	**Sets the Begin device address to hhhh. (121A only)**
H	No operation
/	Returns the decimal number of devices which failed the last operation, followed by the number of sockets with devices in them.
hhΛ	Clear all RAM with data hh (ØØ default).
nn22]	Convert to a 16-bit programmer. nn specifies the number of bits, either 8 or 16.
n23]	Sets the number of verify passes; n is to be either 1 or 2.
n25]	Select Electronic ID options.
hhll18]	Set V_{CC} levels during verify; hh sets the high pass; ll sets the low pass.
DF]	Inquire device status for all 20 sockets.
I/O Commands	
nnn A	Sets the data translation format code to nnn.
I	Inputs data from the serial port.
O	Outputs data to the serial port.
C	Compares data in RAM with data coming in the serial port.
hhhh W	Sets the I/O offset to hhhh. +
=	Disables the I/O timeout.
hh U	Sets the number of nulls after a carriage return to hh, and enables line feeds.

NOTE

The variables hhhh and nnn are used to denote either hexadecimal values (hhhh) or decimal values (nnn) that must be entered.

*Set Programming available only on the 121A.
+ Address offset can be up to 8 characters in some I/O formats.

3.6.4 CONTROL COMMANDS

These are used to execute or suspend a command.

• RETURN — RETURN

Executes each command. It must be sent to the programmer immediately after each command. All commands are ignored if not followed by RETURN.

• ESC or BREAK — ESC or BREAK

Causes the programmer to unconditionally halt (abort) any operation in progress and send the prompt character, <. It will then wait for further instructions.

3.6.5 DEVICE COMMANDS

These commands execute the operations used in device programming.

• ILLEGAL BIT TEST — nn T

Instructs the programmer to test the devices or sets of NN devices (nn = number of devices in a set) for illegal bits. An illegal bit is defined as a programmed bit in the device that does not exist in RAM. **In Set Programming, the default is one device per set.**

• BLANK CHECK — B

Instructs the programmer to search the device(s) for programmed bits.

• SELECT FAMILY AND PINOUT — FFPP @

A 2-digit Family Code (FF) and a 2-digit Pinout Code (PP) are sent to the programmer ahead of this command. This command tells the programmer which devices are to be programmed.

• EEPROM TEST — nnnnnn20]

This command instructs the programmer to execute the EEPROM test. The test will execute nnnnnn times (1 to 999999), where one is the default.

• INSERT PARTS — &

This command instructs the programmer to enter the Insert Parts mode.

The front panel display will display: "INSERT PARTS." This mode will be the same as the Insert Parts mode entered by the front panel. All errors 30-39, 70-89 will be reported to the front panel, and not to the controller. This mode can be exited in any of three ways: (1) pressing the START key on the front panel, (2) successfully inserting all 20 parts, or (3) the controller sending an ESC character. When an error is being displayed, this mode cannot be exited, except by ESC. When exiting by pressing START or inserting 20 parts, the socket will be checked, electronic ID will be performed, and errors will then be reported to the controller. On exiting this mode, the front panel will display: "REMOTE MODE."

• LOAD — L

Instructs the programmer to load data into RAM from a master device, **or set of masters (121A)**

• PROGRAM — nn P

Instructs the programmer to program RAM data into the devices or sets of nn devices and verifies them. In remote control, the program sequence does not include a blank check or illegal-bit test. (Use the B and T commands for these functions.) In Set Programming, the default value is one device per set.

• VERIFY — nn V

Instructs the programmer to compare RAM data with already programmed devices or sets of nn devices. In Set Programming, the default value is one device per set **(121A only).**

• FAMILY AND PINOUT INQUIRY — [

Instructs the programmer to output the Family and Pinout Codes currently in effect.

• RESPOND — R

Instructs the programmer to indicate the status of the device selected by the current Family and Pinout Codes. Data is output in the form AAA/B/C (or AAAA/B/C) to the computer, where A, B, and C are hexadecimal characters. AAA (or AAAA) is the device word limit; B is the word size (4 or 8); C is either VOL or VOH (Ø is for VOH and 1 for VOL.)

• ELECTRONIC IDENTIFIER FAMILY CODE AND PINOUT CODE INQUIRY — CC

Instructs the programmer to output the electronic Identifier family code and pinout codes currently in effect.

• ELECTRONIC IDENTIFIER INQUIRY — CD

Instructs the programmer to output the electronic identifier codes of the installed device.

3.6.6 UTILITY COMMANDS

These commands set or check operating parameters related to many operations.

• CONFIGURATION NUMBER — G

The programmer sends the 4-digit hex number representing the particular configuration of software resident in the programmer.

• SUM-CHECK nnS

When nn is zero (default), this command instructs the programmer to calculate the sum-check of RAM data from the begin RAM Address expressed by the < command to the word limit of the device type or the block size selected.

With nn equal to the socket, the sum-check of a particular device in a set (121A only) is calculated. Socket nn may not be larger than the set size.

The reponse will be a four-digit hexadecimal number, equal to the sum-check of the socket requested.

• CLEAR RAM hhV

This command instructs the programmer to clear all RAM with data hh (ØØ default).

• 16-BIT MODE nn22]

This command is for the 121A only. This mode allows the operator to convert the 121A into a 16-bit programmer. When this mode is in effect, the programmer will perform device-related operations (Load, Program, and Verify) as though each pair of 8-bit-wide PROMs were a single 16-bit-wide device. The number nn specifies the number of bits, either 8 or 16.

• ONE/TWO PASS VERIFY n23]

This command sets the number of verify passes (n) that are to be made. The number n is to be either 1 or 2.

• ELECTRONIC ID OPTIONS n25]

This command allows the electronic ID feature of the 120A/121A to be disabled, and/or the Unsupported ID Warning Message to be inhibited. The number n specifies the conditions as follows:

n	Electronic ID Feature	Unsupported ID Warning Message
Ø (default)	enabled	on
1	enabled	inhibited
2	disabled	off

• VARY V_{CC} hhll18]

This command allows the V_{CC} levels during verify to be changed. The value hh sets the high-pass verify V_{CC} level in tenths of volts (allowable range is 50 to 60). The value 11 sets the low-pass verify V_{CC} level in tenths of volts (allowable range is 40 to 50).

• DEVICE FAILURE STATUS DF]

This command outputs the device status for all 20 sockets. The bits indicate status as follows:

Bit 7	Error
Bit 6	Non-blank error
Bit 5	Unsupported ID warning
Bit 4	Invalid ID error
Bit 3-1	Not used
Bit 0	Device present

The response to the controller will be 20 two-digit hexadecimal numbers, each followed by a space.

• ERROR CODE INQUIRY X

Instructs the programmer to output the last error codeswhich occurred. The command also clears the error codesfrom memory. Error code information appears at the end of this section. Up to 16 errors are stored.

• DEVICE ERROR STATUS /

Instructs the programmer to output XX-YY, where
XX = Number of devices that failed
YY = Number of devices in sockets

• BEGIN RAM ADDRESS (121A) hhhhhh<

This command, preceded by a 6-digit hex address (hhhhhh), sets the first RAM address to be used for data transfers. The default value is Ø.

• BLOCK SIZE hhhhhh;

This command, preceded by a 6-digit hex value (hhhhhh), sets the number of bytes to be used in data transfers. Any word limit in effect is overridden. With the block size set less than, or equal to, the word limit of the device, the number of bytes moved will be equal to the block size times the number of devices in the set. The number of bytes moved will be equal to the block size, if the block size is greater than the device size. The default value of the number of bytes moved is the word limit of the selected device times the set size. To reset the block size to the default value, enter Ø.

• BEGIN DEVICE ADDRESS hhhhhh :

This command, preceded by a 6-digit hex address (hhhhhh), sets the first device address from which or to which data is to be transferred. Default value is Ø.

• NO OPERATION H

This is a null command and will always return a prompt.

• EXIT REMOTE CONTROL Z

Returns control to the programmer keyboard; all RAM data and operating parameters are retained.

3.6.7 I/O COMMANDS

This group of commands sets up the programmer to transmit or receive data through the serial port.

- **SELECT TRANSLATION FORMAT** — nnn A

Selects the input or output data translation format expressed by the format code nnn in the command. Appendix A explains the formats in detail. The default value is MOS Technology Format #81. The translation formats are listed in Table 3-6.

- **INPUT DATA** — I

Instructs the programmer to accept formatted data from the computer.

- **OUTPUT DATA** — O

Instructs the programmer to translate RAM data into the selected translation format and output this data to the computer.

- **COMPARE DATA** — C

Instructs the programmer to compare data in RAM with data sent through the serial port from the controlling instrument.

- **DISABLE TIMEOUT** — n=

This command disables the I/O Timeout when n is zero (default). When n is nonzero, the I/O Timeout will be enabled.

- **I/O OFFSET** — hhhhhhhh W

Up to eight hex characters (hhhhhhhh) preceding W specify an address to be subtracted from all addresses input to the programmer and added to all addresses output from it. This allows the adjusting of RAM addresses to the address range of larger memories. The default value is 0000 on output and the first incoming address on input, and can be reset to default by entering FFFFFFFF.

- **SET NULLS** — hh U

Sets the number of nulls after a carriage return on output operations; and enables line feeds. FF number of nulls causes no line feeds and no nulls to be sent after each carriage return.

n Format Codes

FORMAT	CODE
Binary**	10
DEC Binary	11
ASCII-BNPF**	01 (05)* +
ASCII-BHLF**	02 (06)* +
ASCII-BH10F**	03 (07)* +
Spectrum	12 (13)* +
ASCII-Octal (Space)	30 (35)
ASCII-Octal (Percent)	31 (36) +
ASCII-Octal (Apostrophe)	32
ASCII-Octal SMS	37
ASCII-Hex (Space)	50 (55) +
ASCII-Hex (Percent)	51 (56) +
ASCII-Hex (Apostrophe)	52
ASCII-Hex SMS	57
ASCII-Hex (Comma)	53 (58) +
RCA Cosmac	70
Fairchild Fairbug	80
MOS Technology	81
Motorola Exorciser	82
Intel Intellec 8/MDS	83
Signetics Absolute Object	85
Tektronix Hexadecimal	86
Motorola Exormax	87
Intel MCS-86	88
HP 64000 Absolute	89
Texas Instruments SDSMAC	90

*For transmission of data without start codes, these alternate format codes are used.

**I/O Offset inoperable

+ For transmission of data with the SOH (CNTL A) start code, these alternate format codes are used.

3.7 ERROR CODES

Table 3-7 lists the programmer's error codes. The display, meaning and corrective actions are given for each.

Table 3-7. Error Codes

DISPLAY	DESCRIPTION	CORRECTIVE ACTION
NO SUCH PN 01	The file part number cannot be located on the disk in either drive.	Check to be sure you have the right disk and that the correct part number was entered.
PN IS USED 02	An attempt was made to create a file using a part number already used on that disk.	Check whether the part number is correct.
NO DISK Ø4	No disks in the drives or the door to a drive is open.	Check the disk drives.
NO CONT SECT Ø5	The empty blocks left on the disk are too small to store the file in 28 sectors. The DCU will not break up a file into more than 28 sectors.	Insert a new data disk.
SINGLE DRIVE 06	An operation requiring 2 drives was attempted on a DCU with only one drive.	Buy a DCU with 2 drives.
DISK FULL Ø7	Not enough room left on the disk to store the file.	Insert a new data disk to store the file.
WRITE PROTECT Ø8	An attempt was made to store a file on a write-protected disk.	Remove the write-project tab from the disk or insert a new diskette.
DISK ERROR Ø9	The disk allocation map is faulty.	Usually caused by a bad diskette. Replace diskette.
DISK ERROR 10	The track was not found.	Usually caused by a bad diskette. Replace diskette.
DISK ERROR 11	CRC error; disk data won't read back corrected.	Usually caused by a bad diskette. Replace diskette.
DISK ERROR 12	Sector not found.	Usually caused by a bad diskette. Replace diskette.
DISK ERROR 13	Lost data; problem with the DCU hardware.	Troubleshoot the DCU.
DISK ERROR 14	Write fault; problem with the DCU hardware.	Troubleshoot the DCU.
FILE VFY ERR 15	The data in the programmer RAM failed to verify with the data in the specified file.	Reload data into RAM. If the problem persists, service the programmer or notify your local Data I/O Service Center.
DCU I/O ERR 16	Data is not being transmitted between the programmer and the DCU.	Check connections between the programmer and the DCU.
DISK IS BAD 17	The disk inserted is defective.	Replace faulty diskette.
DISK FORM ERR 18	The DCU was unable to format the disk in drive 1.	Either there is a problem with the DCU hardware, or the disk is of the wrong kind (i.e., disks must be soft sectored).

Table 3-7. Error Codes (Continued)

DISPLAY	DESCRIPTION	CORRECTIVE ACTION
DISK COPY ERR 19	An error was encountered while trying to copy one or more of the files during a copy disk command.	Determine which files did not get copied. Then, try to transfer the information by using the Copy File Select function to isolate the proglem.
NONBLANK 20	Device failed the blank test.	Press START to override.
ILLEGAL BIT 21	Not possible to program the device due to already programmed locations of incorrect polarity.	Erase the device if possible or discard it.
EEPROM FAIL 22	Device failed EEPROM Test.	Replace device, if faulty.
BAD DEV CODE 25	An incorrect Family and Pinout code was entered.	Consult the Family and Pinout code table of the Operator Guide or Table 1-1 of this manual for the correct code. Then enter the correct code.
WRONG SOCKET 26	The PROM was inserted in a socket which could make the outcome of the operation ambiguous.	The PROM should be removed from the indicated socket.
BLOCK LIM ERR 27	PROM or RAM size is insufficient for the current operation as specified by Begin RAM, Block Size or Set Size.	Check Begin RAM, Block Size or Set Size to be sure they are set correctly. Select Code 10 will display how much working RAM you have. You may need more RAM, or need to have your RAM serivced.
BYTCNT TOO HI 28	The byte count, as set, exceeds the device size or RAM size.	Check byte count for appropriate value.
VERIFY ERROR 29	The programmed PROM data failed to verify against the master data in RAM.	Reprogram the device, if possible; or, insert and program a new part.
ODD LOAD ERR 30	Loaded odd number of devices for 16-bit mode.	Load set with even number of devices.
NOT TRISTATE 31	Device failed to TRI-STATE™ all data pins.	Indicates device is faulty.
DEV NOT EN 32	All the device's data pins are not driving when the chip is enabled.	Indicates device is faulty.
DATA SHORT 33	The device contains a short on its data line.	Insert a valid device.
ADDRESS SHORT 34	The device contains a short on its address line.	Insert a valid device.
NOT TRISTATE 35	Device failed to TRI-STATE™ when deselected.	Indicates device is faulty.
BAD INSERTION 36	The device was inserted into the socket incorrectly.	Align the device in the proper manner and reinsert it in the socket.
BYTCNT TOO LO 37	Byte count is less than ten for a 3-voltage part.	Set byte count to ten or more when programming 3-voltage parts.

Table 3-7. Error Codes (Continued)

DISPLAY	DESCRIPTION	CORRECTIVE ACTION
OVERCURRENT 38	The device to be programmed is drawing excessive current.	One of the devices is faulty.
FRAME ERR 41	The serial interface detected a start bit but the stop bit was incorrectly positioned.	Check the baud rate and stop bit switches.
OVER RUN ERR 42	The serial interface received characters when the programmer was unable to service them.	Check connections. Handshake lines may not be properly connected.
PARITY ERR 43	The incoming data has incorrect parity.	Check the parity switch and try again.
ERROR 44	Unidentifiable Interrupt Request	Contact your nearest Data I/O Service Center
I/O TIMEOUT 46	No characters (or only nulls and rubouts) were received on serial input for 25 seconds after pressing the START key, or no characters could be transmitted for a period of 25 seconds due to the state of the handshake lines.	Check all connections, then restart operation.
FIFO OVERFLOW 47	The main Serial Port FIFO is in an overflow condition.	Check connections. Handshake lines may not be properly connected.
FIFO OVERFLOW 48	The command FIFO is in an overflow condition.	Check connections. Handshake lines may not be properly connected.
FIFO OVERFLOW 49	The FIFO that interfaces with the second serial port is in an overflow condition.	Check connections. Handshake lines may be properly connected.
I/O FORM ERR 51	The programmer received an invalid address field.	Check the connection of units in the system, data format, and data source, and then try again.
I/O VFY FAIL 52	The data from the serial port did not match the data in RAM.	Reload data into RAM. If the problem persists, service the programmer or notify your local Data I/O Service Center.
I/O FORM ERR 53	The number of input records did not equal the Record Count. (MOS Technology Format only.)	Check the connection of all units in the system, data format, and data source, and then try again.
I/O FORM ERR 54	The record type was in error. (Intel-Intellec 8/MDS Format only.)	Check the connecti of all units in the system, data format, and data source, and then try again.
I/O FORM ERR 55	The sum-check field received by the programmer does not agree with its own calculated sum-check.	Check all connections of units in the system, data format, and data source, and then try again.
I/O FORM ERR 56	The address field encountered on data input is outside the range of RAM addresses.	Enter the correct value during input operation.
I/O FORM ERR 57	Data sent to the programmer are non-hexadecimal characters.	Input data in the correct format.

Table 3-7. Error Codes (Continued)

DISPLAY	DESCRIPTION	CORRECTIVE ACTION
I/O FORM ERR 58	The address check was in error.	Check all connections of units in the system, data format, and data source, and then try again.
NO RAM 61	There is no working RAM in the programmer.	Replace faulty RAM or have the programmer serviced by your nearest Data I/O Service Center.
RAM IS BAD 62	The programmer RAM is defective.	Replace faulty RAM or have the programmer serviced by your local Data I/O Service Center.
RAM WRITE ERR 63	The programmer is unable to write the intended data in RAM	Failure of the associated RAM chip; replace the failed chip.
RAM DATA ERR 64	The programmer detected an invalid change in RAM data.	Reload data into RAM. If the problem persists, service the programmer or notify your local Data I/O Service Center.
RAM IS BAD 65	The programmer RAM is defective.	Replace faulty RAM or have the programmer serviced by our local Data I/O Service Center.
PORT IS BAD 66	The main serial port is faulty.	Contact your local Data I/O Service Center.
DATA COMP ERR 67	A self test routine indicates that the programmer's data comparators are faulty.	Contact you local Data I/O Service Center.
TIMER IS BAD 68	During the self test routine, the programmer's timing chip failed to respond.	Contact your nearest Data I/O Service Center.
DATA TEST ERR 69	Self test indicates that the programmer's data latches are faulty.	Contact your nearest Data I/O Service Center.
PIN 1 ERROR 71	Self test indicates that the socket pin 1 driver is at an inaccurate level.	Contact your nearest Data I/O Service Center.
PIN 2 ERROR 72	Self test indicates that the socket pin 2 driver is at an inaccurate level.	Contact your nearest Data I/O Service Center.
PIN 20 ERROR 73	Self test indicates that the pin 20 driver is at an inaccurate level.	Contact your nearest Data I/O Service Center.
PIN 21 ERROR 74	Self test indicates that the socket pin 21 driver is at an inaccurate level.	Contact your local Data I/O Service Center.
PIN 22 ERROR 75	Self test indicates that the socket pin 22 driver is at an inaccurate level.	Contact your local Data I/O Service Center.
PIN 23 ERROR 76	Self test indicates that the socket pin 23 driver is at an inaccurate level.	Contact your local Data I/O Service. Center.

Table 3-7. Error Codes (Continued)

DISPLAY	DESCRIPTION	CORRECTIVE ACTION
PIN 26 ERROR 77	Self test indicates that the socket pin 26 driver is at an inaccurate level.	Contact your local Data I/O Service Center.
PIN 27 ERROR 78	Self test indicates that the socket pin 27 driver is at an inaccurate level.	Contact your local Data I/O Service Center.
PIN 28 ERROR 79	Self test indicates that the socket pin 28 driver is at an inaccurate level.	Contact your local Data I/O Service Center.
NO ID FOUND 81	Device has no electronic ID.	Check the device type. Consult the Family and Pinout code table of the Operator Guide or Table 1-1 of this manual for the correct code. Then enter the correct code.
INVALID ID 82	Device's electronic ID is incompatible with the Family and Pinout codes selected.	Remove the device.
ID WARNING 83	Device's electronic ID is unknown to the programmer.	Check the device type. Consult the Family and Pinout code table of the Operator Guide or Table 1-1 of this manual for the correct code. Then enter the correct code. If the Family and Pinout codes are correct, press START to continue. This warning message can be disabled by Select Code 25.

SECTION 4
TROUBLESHOOTING

4.1 INTRODUCTION

The following troubleshooting information is an aid to understanding malfunctions and locating programmer hardware failures. Section 2 helps to determine the type of trouble in the unit and the steps that are necessary for further servicing.

4.2 PRELIMINARY TROUBLESHOOTING

The following paragraphs describe some of the common problems, with corrective steps following each. After performing each step, determine whether the problem still exists.

4.2.1 PROGRAMMER DOES NOT OPERATE OR OPERATES ERRATICALLY

1. Check the CORCOM voltage selector card against the line voltage. These voltages should be the same. If not, refer to section 2.3.1 for changing the voltage selection card. For proper operation, the line voltage must be within +5% −10% of the voltage shown inside the window.
2. Check that the AC power cord is firmly plugged in and the power switch is on.
3. Check that the socket boards are properly cabled.
4. Remove any cables attached to the serial interface. If the programmer then works properly, there is a problem with your serial interface. In this case, contact your nearest Data I/O Service Center.
5. Check that the programmer is within operating specification by following the troubleshooting procedure in paragraph 4.3.2.
6. Check the installation of all hardware. Check the orientation and connections of all cables as well as the seating of all circuit boards.
7. If steps 1 through 6 do not reveal the problem, contact your nearest Data I/O Service Center.

4.2.2 SERIAL I/O FAILURES

1. Make sure the programmer and other equipment to which its attached are set for the same parity, baud rate and number of stop bits.
2. Check the operation of the peripheral equipment according to the manufacturer's procedures.
3. If steps 1 and 2 do not reveal the problem, contact your nearest Data I/O Service Center.

4.3 TROUBLESHOOTING SPECIFIC AREAS

The programmer contains a special troubleshooting mode that allows the user to test specific areas of the programmer to isolate hardware malfunctions. The tests are identified and described in Table 4-1.

4.3.1 ENTERING THE TROUBLESHOOTING MODE

To enter the troubleshooting mode:

1. Turn segment 6 of U4 on the Specific I/O card to the ON position. Refer to Figure 2-6.

CAUTION

While in the troubleshoot mode, device related operations may be attempted to check waveforms, but do not insert devices into sockets. Once the troubleshoot mode switch has been activated, according to the instructions in Step 1, all operations require the password (SHIFT 2/BACKSPACE).

2. Press SELECT. Display: SEL FUNCTION -<
3. Enter password.
4. Enter 12. Display: TROUBLESHOOT 12
5. Press START. Display: SEL TEST -<
6. Now decide which test(s) you want to use. A description of each test is provided in Table 4-1. Once you have selected the test(s) refer to the following section for your test procedure.

4.3.2 USING THE TROUBLESHOOTING MODE

The troubleshooting mode allows you to test nine different areas of the programmer. The tests that you select depend on what areas you suspect are not working properly. Generally, error code information is a starting point from which to select a test. The following procedures explain how to use each individual test.

Address Loop - Test 01

1. With the programmer in the troubleshooting mode, enter 01.
2. Press START. Display: ADDRESS LOOP.
3. Trigger your oscilloscope on each address pin socket (Refer to Figure 4-1.) You should observe waveforms of uniform height and width.

Address Test - Test 02

1. With the programmer in the troubleshooting mode, enter 02.
2. Press START. Display: ADDR - XXXX<.
3. Enter the address, in hexadecimal, that you want to test.
4. Press START. Display: ADDR - XXXX<.
5. Return to step 3 if you wish to select another address.

Data At Socket - Test 03

1. With the programmer in the troubleshooting mode, enter 03.

2. Enter the socket number that you want to drive data on. (Entering a Ø at this step activates a dynamic test on all sockets at one time.)
3. Press START. Display: SOCKET - XX D-YY<.
4. Enter data (YY).
5. Press START. Display: SOCKET - XX D-YY<.
6. If you wish, enter new data.
7. Press START.
8. If you wish to test a different socket, press SELECT and return to step 2.

Driver Pin - Test 04

1. With the programmer in the troubleshooting mode, enter 04.
2. Enter the driver pin number.
3. Press START. Display: PIN XX - +XX.XV L-1
4. Press START. Display: PIN XX - +XX.XV L-2
   In other words, pressing START repeatedly allows you to increment through the voltages and levels listed in Table 4-2.
5. If you wish to test another driver pin, press SELECT and return to step 2.

Table 4-1. Troubleshooting Tests

TEST	NUMBER	DESCRIPTION
Address Loop	01	This test allows the technician to check the address lines for possible shorts or overload conditions by applying a 200 us low pulse on all address lines, one at a time, in the following order: pins 10, 9, 8, 7, 6, 5, 4, 3, 25, 24, 2, and 27.
Address Test	02	Specifies the programmer address that you want tested. The address that you key in will be sent to the sockets. The programmer will read back and display this address. The value you keyed in - and the displayed value - should be the same.
Data at Socket	03	This test allows you to select data and drive it to the socket of your choice. The programmer will read back and display the data. The data entered and the data displayed should be identical.
Driver Pin	04	This test allows you to troubleshoot the selected driver pin. Figure 4-1 shows the location of the driver pins. The display will show the selected driver pin number, the voltage and the voltage level number. The display value should correspond to the information in Table 4-2. If you wish, you can measure the voltage at the selected driver pin by connecting up a Digital Volt Meter to the pin that you selected.
Loop On Pin	05	This test allows you to measure the voltage at the pin that you select from Table 4-2. This test causes the pin's voltage to continually switch from the level 1 to level 4. The voltage for levels 2 and 3 do not apply to this test. The voltage will stay at level 1 for 4.5 ms, then it will switch to level 4 for 4.5 ms and back to level 1 to repeat the process. The "loop" will continue until a new test is selected. This test is helpful in testing rise times, overshoot, and other switching conditions.
Ramp Pin	06	This allows you to select a pin and then ramp its voltage from level 1 to level 4. This test is different from Test #5 because the ramp includes levels 3 and 4. By triggering your scope off the selected pin, a smooth ramp pattern should appear.
LED Test	07	This test checks the socket panel's LEDs. Each depression of the START key activates an LED in numerical order. A "00" display means LEDs are not activated. A "21" means all LEDs should be lit.
RAM Test	08	This test checks the programmer's RAM. When the test is completed, the programmer displays two addresses: the last address to correctly store a hex 55 pattern, and the last RAM address which successfully completed the entire RAM test.
Loop On	09	Causes the processor to continuously write to and read a zero from the entered address on the processor bus. The purpose of this test is to make sure the circuitry is decoding properly.

Loop On Pin - Test 05

1. With the programmer in the troubleshooting mode, enter 05.
2. Enter driver pin number.
3. Attach scope to pin socket.
4. Press START. DISPLAY: LOOP ON PIN - XX<
5. If you wish to test another pin, press SELECT and return to step 2.

RAMP Pin - Test 06

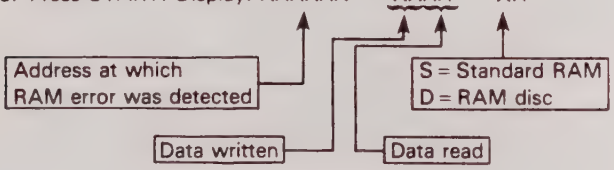
1. With the programmer in the troubleshooting mode, enter 06.
2. Enter driver pin number that you want to test.
3. Press START. Display: RAMP PIN - XX.
4. If you wish to test another pin, press SELECT and return to step 2.

LED Test - Test 07

1. With the programmer in the troubleshooting mode, enter 07.
2. Press START. Display: LED TEST - XX.
3. If you wish to increment through the LEDs, press START.

RAM Test - Test 08

1. With the programmer in the troubleshooting mode, enter 08.
2. Press START. Display: RAM TEST.
3. Press START. Display: XXXXXX XXXX X^



4. Press SHIFT 1. Display: Same as for step 3 above.
5. Press START to continue the test or to start the test over.

Loop On Address - Test 09

1. With the programmer in the troubleshooting mode, enter 09.
2. Enter address.
3. Press START. Display: LOOP ON - XXXX.
4. If you wish to change the address, press SELECT and return to step 2.

Table 4-2. Voltage Levels for Troubleshooting Tests 04, 05 and 06

Pin Number	Level 1 Volts	Level 2 Volts	Level 3 Volts	Level 4 Volts
1	0	5.0	17.0	25.0
20	0	5.0	17.0	26.0
21	0	4.5	5.5	12.5
22	0	5.0	17.0	26.0
23	0	-5.0	5.0	25.0
26	0	4.5	12.5	5.5
28	0	4.5	5.5	12.5

Tolerances:
Programmer Display: Listed Voltage ± 0.3V
DVM Display: Listed Voltage ± 0.1V

4.3.3 AFTER TROUBLESHOOTING

After finishing the troubleshooting tests, make sure you return segment 6 of U4 on the specific I/O card to the OFF position. Refer to Figure 2-6 for the location of U4.

4.3.4 EXITING THE TROUBLESHOOTING MODE

You may exit the troubleshoot mode at any time. Simply press any of the mode keys (LOAD, PROG, VERIFY or SELECT.)

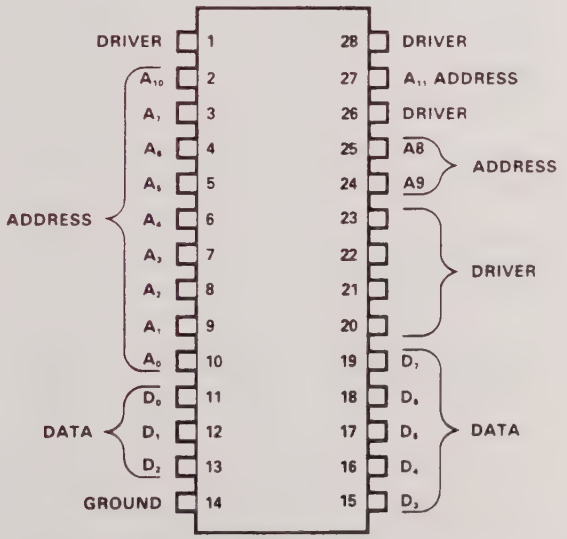


Figure 4-1. Troubleshoot mode - Pin Assignments

SECTION 5
CALIBRATION

5.1 INTRODUCTION

Calibration is normally not required because high-precision components keep the programmer within specification. The information in this section is intended to provide you with a way of verifying the performance of your programmer and, if necessary, of calibrating it.

Typically you would need to calibrate if:

- You are not receiving the proper programming yields and, based on your observation of waveforms, you suspect out-of-calibration performance.
- Your company policy requires periodic calibration;
- You replace a high-precision component; or if
- The programmer fails the verification procedure in this section.

5.2 PERFORMANCE VERIFICATION

The Performance Verification Check procedure, which follows, provides a quick way to check out the operating condition of the programmer.

You will need the following tools to accomplish this procedure:

- Digital Voltmeter (Fluke 8000A or equivalent)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

The following is a step-by-step performance verification of your programmer.

5.2.1 Entering Performance Verification Mode

In the following steps where a digital voltmeter (DVM) is required, the negative lead is always connected to ground at pin 14 of the socket being measured.

Before executing any of the following tests, make sure you have removed the top cover. Refer to the instructions in Figure 2-2.

1. Enter the Troubleshooting mode by turning segment 6 on U4 on the Specific I/O Card (701-1835) to the ON position. Refer to Figure 2-6.

CAUTION

Turn this switch off when you are finished with the tests. Failure to turn off switch could damage parts.

2. Press SELECT. Display: SEL FUNCTION-<
3. Enter password (SHIFT 2/BACKSPACE)
4. Enter 12. Display: TROUBLESHOOT 12
5. Press START. Display: SEL TEST-<

Now you are ready to begin the performance verification tests. The names and locations of the individual pins you will need to probe are listed in Figure 5-1.

5.2.2 Pin Driver Test

All correct voltage values for this test are listed in Table 5-1. Follow the steps in 5.2.1 so that the display reads: SEL TEST-<

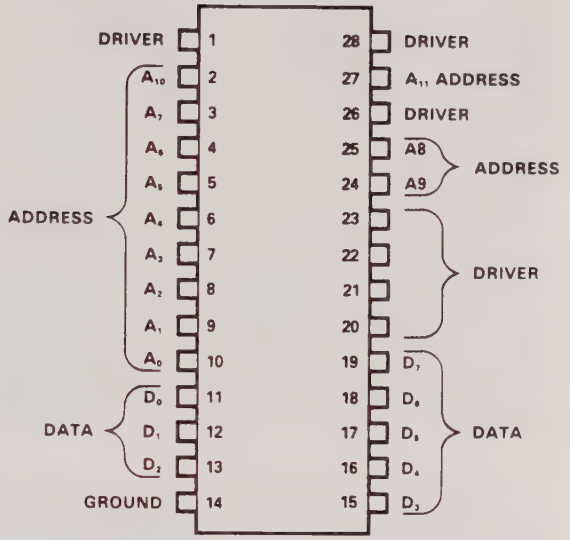


Figure 5-1. Pin locations and designations for Performance Verification Tests

1. Enter 4 (selects pin driver test).
2. Press START. Display: DRIVER PIN 00<
3. Enter 1 (or, number of pin being tested)
4. Press START. Display: PIN 01 - +00.0V L-1
5. Connect the positive lead of your DVM to pin 1 of any socket. Verify that your DVM voltage display corresponds to the value in Table 5-1. The programmer display should show the same value within a tolerance of ± .3V.
6. Press START to change voltage verification level. Once again, verify your DVM reading against Table 5-1 and the programmer display.
7. Once you have verified the voltages for pin 1, continue testing the other driver pins listed in Table 5-1. Press SELECT first. Then repeat steps 3 through 6 entering the correct pin number in step 3.
8. If a voltage that you read at the socket does not correspond to the value listed in Table 5-1, refer to the adjustment procedures in Section 5.3.

5.2.3 Address Test

Follow the steps in 5.2.1 so that the display reads: SEL TEST-<

1. Enter 2 (selects address test).
2. Press START. Display: ADDRESS TEST
3. Press START. Display: ADDR-0000<
4. Enter 555
5. Press START. Display should show 0555.
6. Connect the positive lead of your DVM to each of these pins: 2, 4, 6, 8, 10, 25. Each of these pins should be high (+5 volts, ± .4V.)
7. Connect the DVM's positive lead to each of the following pins: 3, 5, 7, 9, 24, 27. Each of these pins should be low (Ø volts, ± .4V.)

8. Enter AAA. Press START. Display: AAA.
9. Measure the voltage states of the pins in steps 6 and 7. The voltage levels of these steps should be reversed (i.e. pin 2 is now low, and pin 3 is high) (pin 24 5 volts ± 0.7V).

5.2.4 Data at Socket Test

Follow the steps in 5.2.1 so that the display reads: SEL TEST-<

1. Enter 3 (selects data at socket test).
2. Press START. Display: DATA SOCKET-00<
3. Enter 1 (socket 1).
4. Press START. Display: SOCKET-01 D00<
5. Enter 55.
6. Press START. Display: DATA SOCKET-01 D55<
7. Connect the positive lead of your DVM to each of the following pins: 11, 13, 16 and 18. At each pin you should be able to measure +5V (± .4V). Then connect your positive lead to pins 12, 15, 17 and 19. These pins should be at ØV ± .4V.
8. Return to Step 5 and enter AA. Now press START. The display should read: AA. At step 7, measure the voltage states. The voltages at these pins should now be reversed (i.e. pin 11 is ØV and pin 12 is +5V.)

Repeat steps 2 through 8 so that you have tested the data lines for all 20 sockets on the programmer.

5.2.5 Ramp on Pin

Follow the steps in 5.2.1 so that the display reads: SEL TEST-<

1. Enter 6 (selects ramp on pin test).
2. Press START. Display: RAMP PIN-00<
3. Enter driver pin number that you want to test.
4. Attach scope to driver pin.
5. Trigger internally on negative edge of waveform. Delayed sweep will provide optimum display.
6. Press START. Display: RAMP PIN - XX
7. Observe voltage ramp. Ramp should correspond to the waveforms illustrated in Figure 5-2; however, you can expect to see occasional negative going glitches during the ramp. The glitches are a normal occurance, a characteristic of the DACs.
8. If you wish to test another pin, press SELECT and return to step 2.

Table 5-1. Driver Pin Voltage Levels

Pin Number	Level 1 Volts	Level 2 Volts	Level 3 Volts	Level 4 Volts
1	0	5.0	17.0	25.0
20	0	5.0	17.0	26.0
21	0	4.5	5.5	12.5
22	0	5.0	17.0	26.0
23	0	-5.0	5.0	25.0
26	0	4.5	12.5	5.5
28	0	4.5	5.5	12.5

Tolerances:
Programmer Display: Listed Voltage ± 0.3V
DVM Display: Listed Voltage ± 0.1V

CAUTION

If you are now finished with the tests, remember to turn switch 6 (on U4) on the Specific I/O Card to the off position. Refer to Figure 2-6.

5.3 ADJUSTMENT PROCEDURE

If you find that a pin driver voltage does not correspond to the information listed in Table 5-1, adjust the voltage according to the procedure that follows.

You will need the following tools to complete the adjustment procedure:

- Flathead screwdriver (or suitable tool for adjusting small potentiometers.)
- Phillips screwdriver
- Digital voltmeter (minimum: 3 1/2 digits)

To adjust the pin driver voltages, execute the following steps:

-Turn Off Power-

1. First, remove the top cover as illustrated in Figure 2-2.
2. Remove the socket panel. Refer to Figure 5-3 for instructions and an illustration.
3. Stand the socket panel on end. Refer again to Figure 5-3.

CAUTION

Do not remove any cables from their connectors. By bracing the socket panel when standing it on end, you can help avoid the need for cable removal.

-Turn On Power-

4. Enter the troubleshooting mode as you did for the Pin Driver Verification Test. Step through the test to Level 4 for each pin driver.
5. Using your DVM, monitor all voltage levels at the socket pin indicated in Table 5-2.
6. Adjust the potentiometers (locations are given in Figure 5-4), for each pin driver, to the voltage level listed in Table 5-2. All potentiometers adjust in a clockwise direction for increasing voltage.
7. Once you have adjusted the potentiometer for each pin driver, turn off power.

CAUTION

Remember to turn segment 6 (of U4) on the Specific I/O Card to the off position. Refer to Figure 2-6.

8. Reattach the socket panel according to the instructions in Figure 5-3. And, reattach the top cover according to Figure 2-2.
9. Complete, one more time, the Performance Verification procedure described in Section 5.2.1 to insure that your machine is working properly.

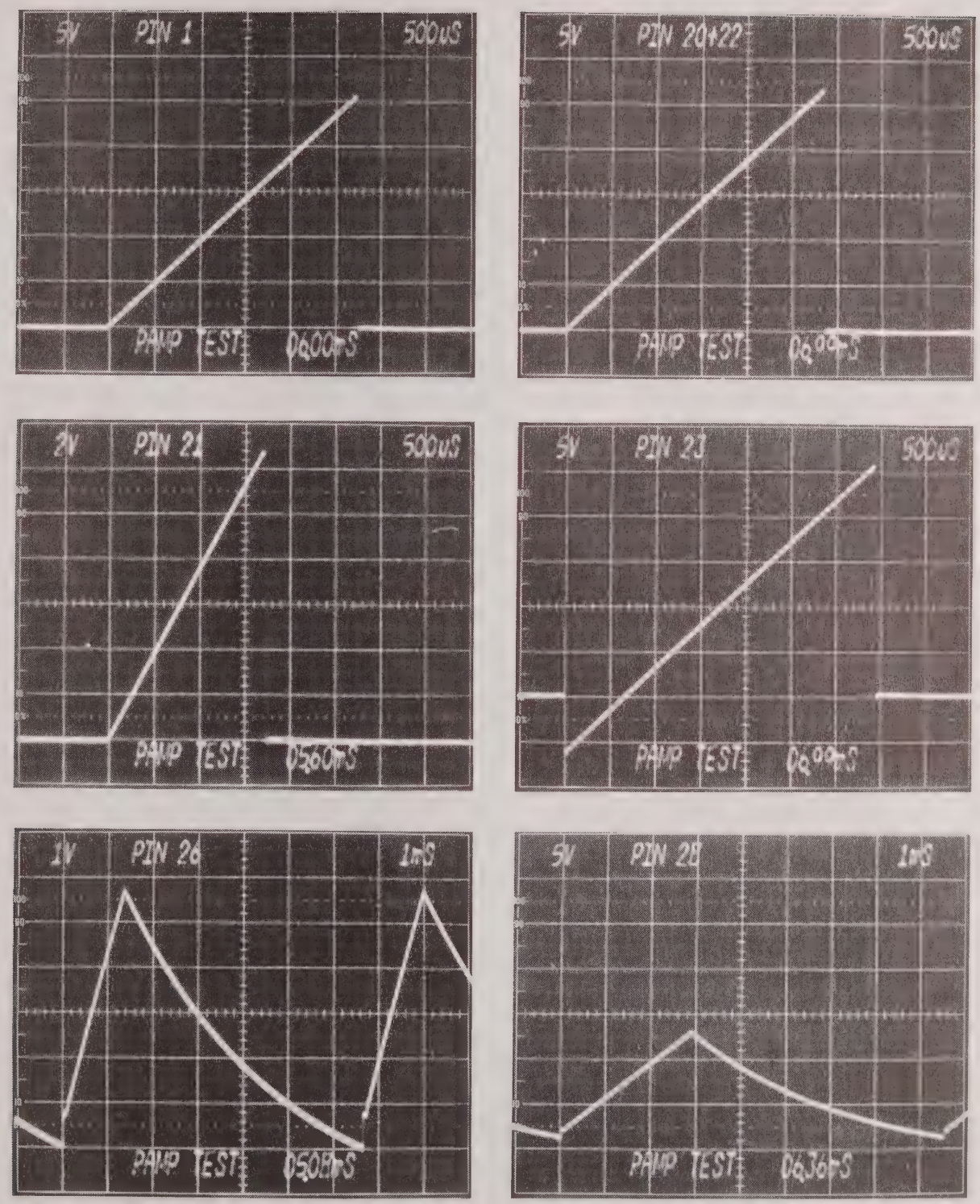
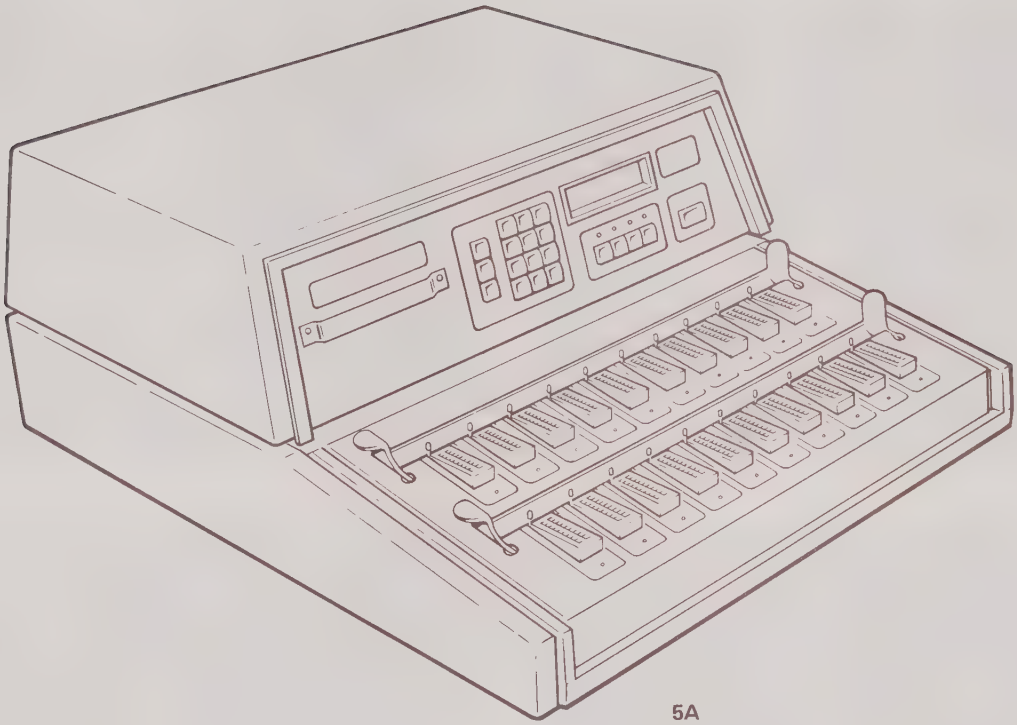
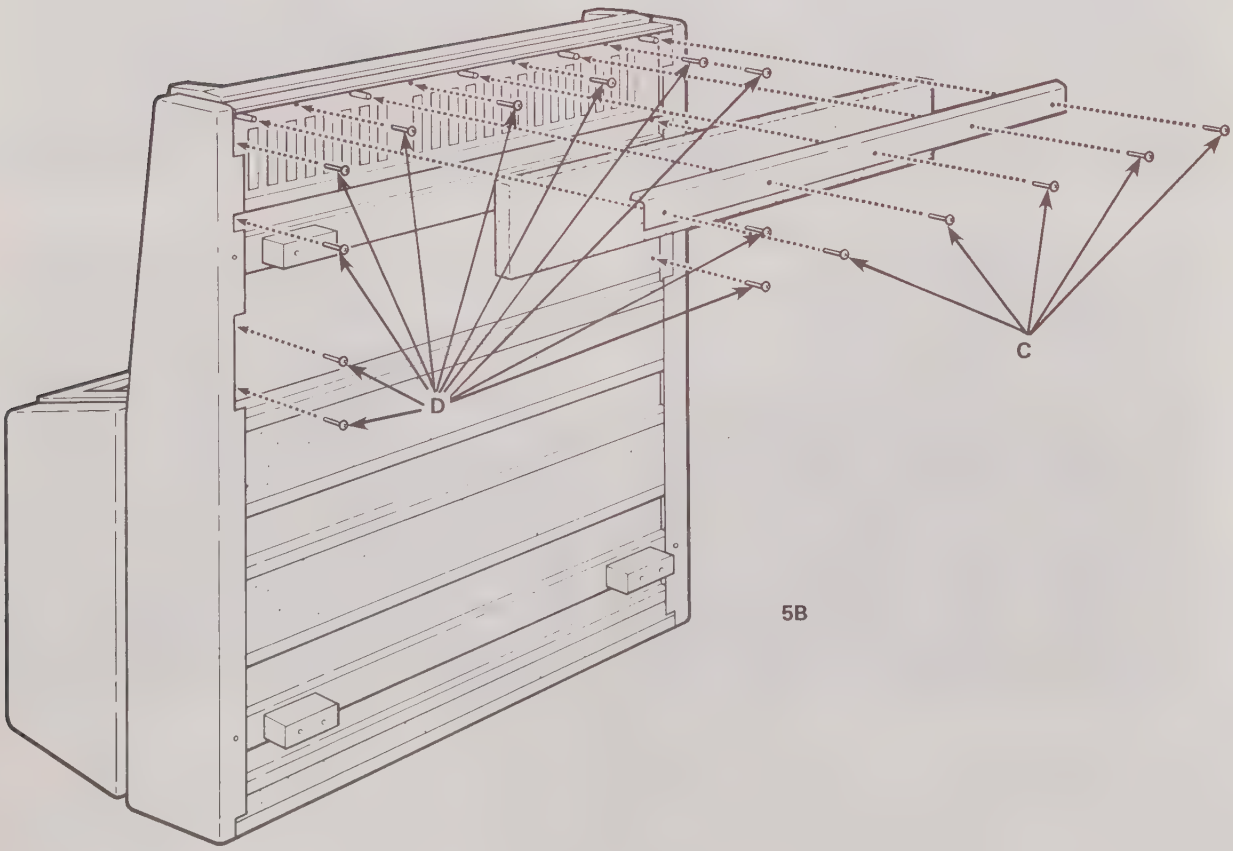


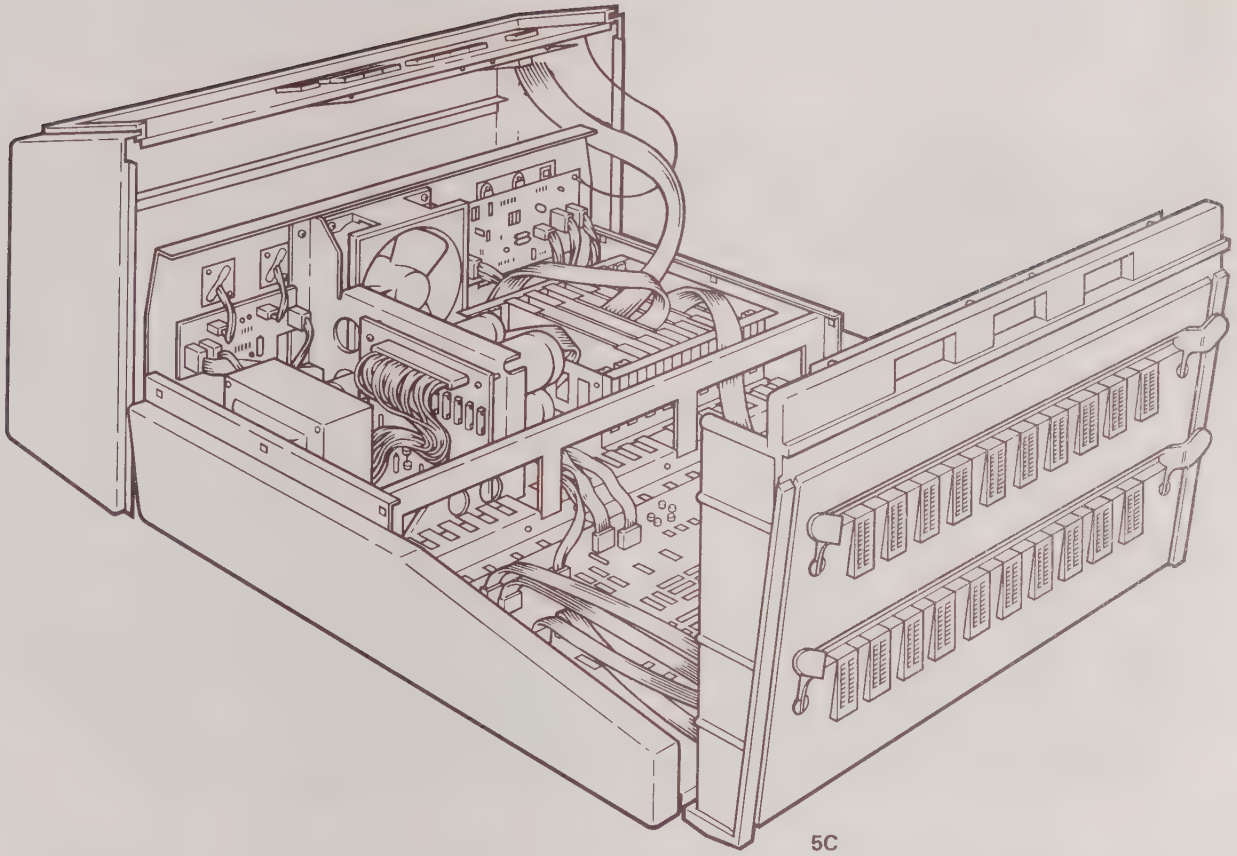
Figure 5-2. Ramp On Pin Test Waveforms



5A



5B



5C

To Remove the Socket Panel:

1. Tip the programmer on end as shown in 5B.
2. Unscrew the (5) screws labeled with a "C". Remove the bracket and foam filter.
3. Remove the (12) screws labeled "D".
4. Return the programmer to its original position as shown in 5A.
5. Lift the socket panel toward you as shown in 5C.
6. Prop the socket panel into a 90° angle respective to the programmer.

Figure 5-3. Disassembly of Socket Panel

Table 5-2. Pin Driver Voltage Levels

Pin Number	*Voltage Level #4	Adjustment Location (Potentiometer)	Monitor at Socket Pin
0	6.40	R 64	+
1	25.00	R159	1
20	26.00	R 95	20
21	12.50	R 78	21
22	26.00	R124	22
23	25.00	R141	23
28	12.50	R 56	28

\+ Monitor Comparator DAC at TP1. See Figure 5-4 for location.

* Voltage tolerance (except Pin 0) is ±.075V; at Pin 0, tolerance is ±.0075V.

10. If you find that your machine is still not delivering the proper programming yields, contact your nearest Data I/O Service Center.

5.4 WAVEFORM OBSERVATION

Programming waveforms can be observed with an oscilloscope and compared against the Timing Diagrams. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the programmer is performing to the PROM manufacturer's standards.

Since the programmer generates a large number of waveforms and all calibration adjustments are accomplished during DC calibration, we recommend observing waveforms only for commonly used PROMs or PROMs that are presenting yield problems.

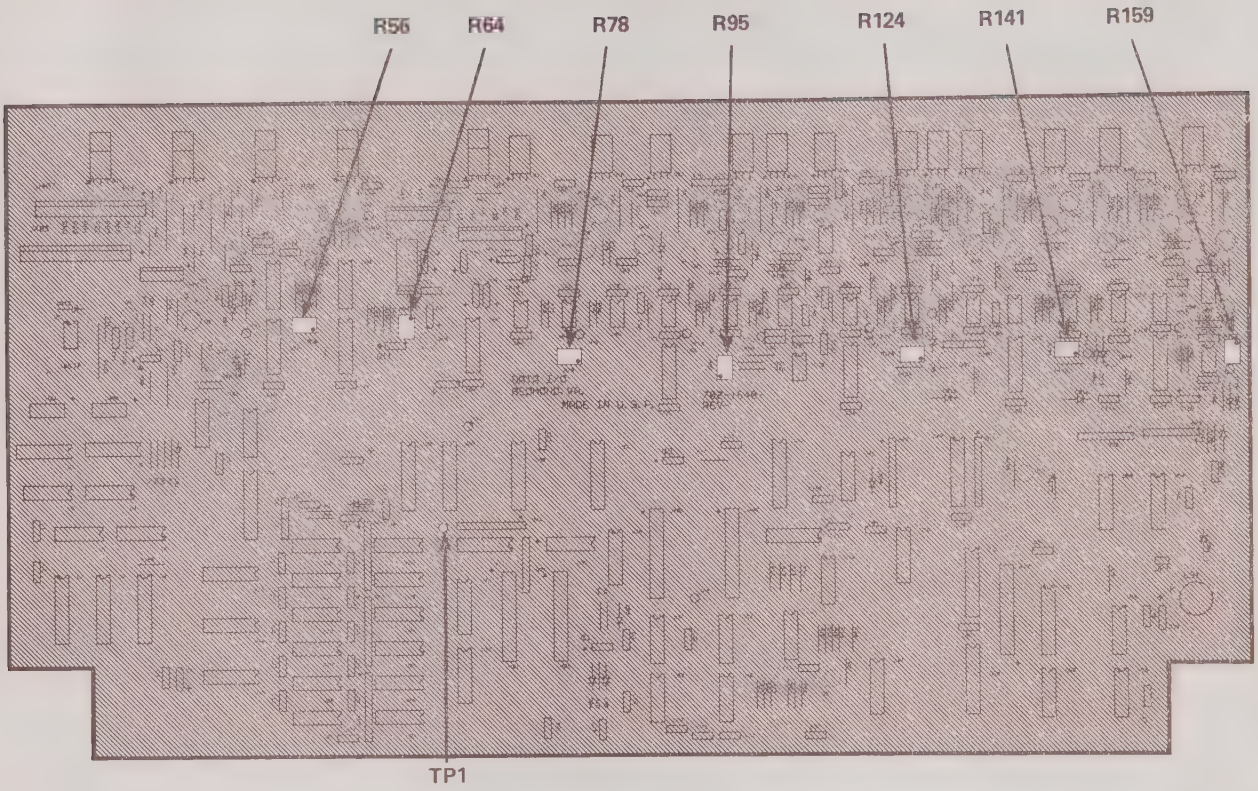


Figure 5-4. Potentiometer and Test Point Locations on the Digital/Analog Driver Board (P/N 702-1640)

5.4.1 The Timing Diagrams

The manual contains a Timing Diagram for each PROM family. Each Timing Diagram contains a set of waveform photographs that show critical programming parameters. The minimum and maximum parameter values are listed in the waveform variables tables on the diagrams. Other voltage and time parameters are to be considered non-critical, with a tolerance of 10%.

For waveform photographs, the trigger was set at the leftmost graticule line; by taking into account any time-base variance, time comparisons can be made between photographs. (The time base is always the same for different waveforms in the same photograph.) Time-base and volt-per-division settings are printed on each photograph.

The waveform names are called out along the left edge of each photograph. Waveform names correspond to the pin names on the Pinout Charts, Figure 5-5. These charts tell which socket contacts to probe when observing the waveforms for a particular PROM pinout within a family.

Detail photographs are included to magnify rapid voltage changes or particular pulses in a pulse train. The delay time is printed at the bottom of each detail photograph. It should be noted that some of the waveform signals appear only once per programming cycle (e.g., VPP rise and VPP fall times).

5.4.2 Observation Procedure

This procedure when used with a Timing Diagram and the Pinout Charts, Figure 5-5, permits waveform observation for any particular PROM-type.

a. Prepare the oscilloscope by connecting the waveform signal (specified beneath the photograph) to the trigger input. Ground the scope to the GND contact (pin 14) of any socket—preferably socket 11.
b. To observe individual waveforms as shown on the Timing Diagram, refer again to the Pinout Charts.
c. Load RAM with either random data or the data specified. The quantity of data should be at least equal to the word limit of the device being observed.
d. Refer to Table 1-4 to determine the Family and Pinout Codes of the selected PROM type.
e. To key in the Family Code and Pinout Code:
   1. Press PROG. Display: PROGRAM PARTS.
   2. Press START. Display: F<
   3. Key in Family and Pinout Codes. Display: FXX PYY<
   4. Press START. Display: INSERT PARTS
   5. Press START to initiate program cycle.
f. Observe waveforms.

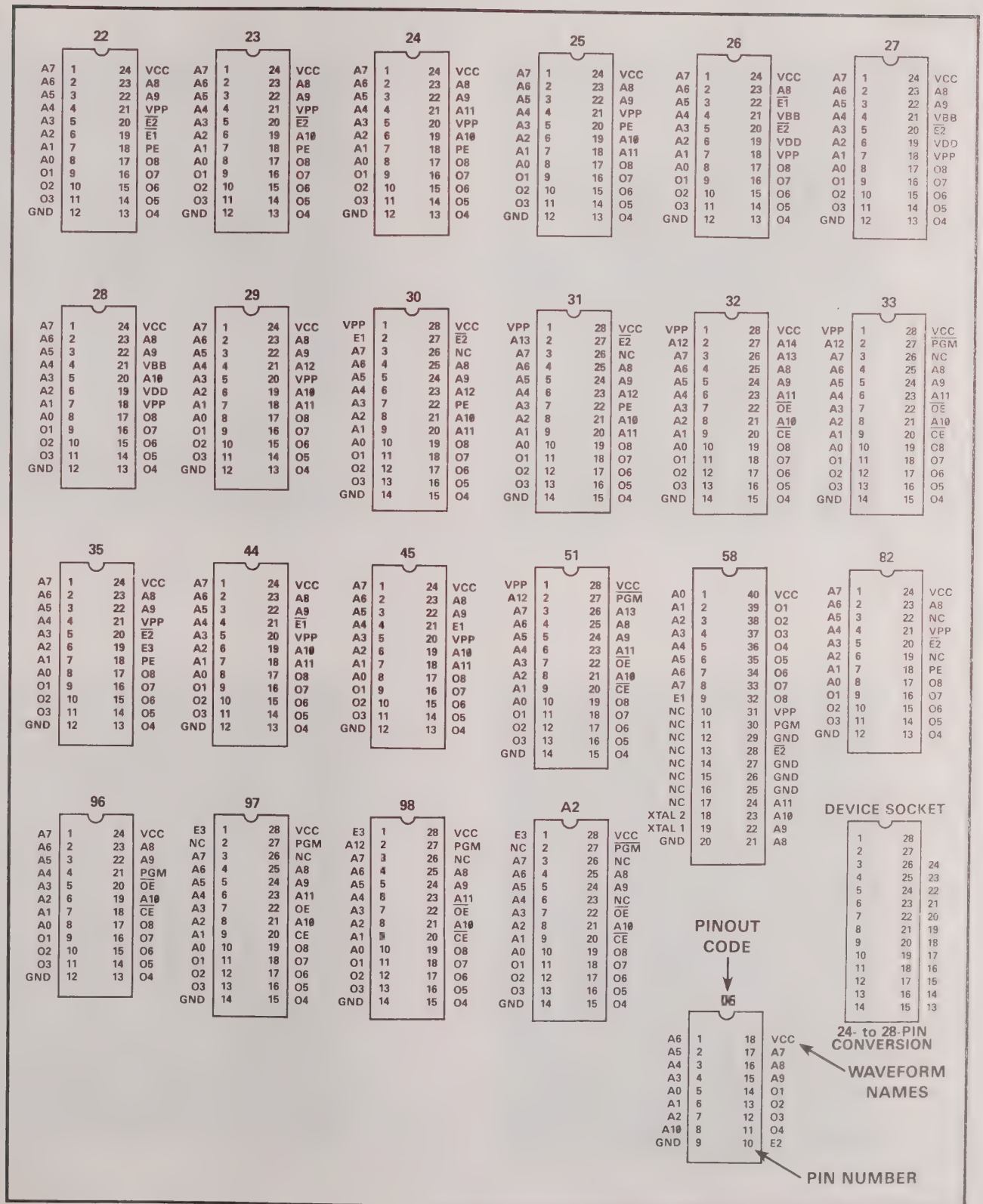
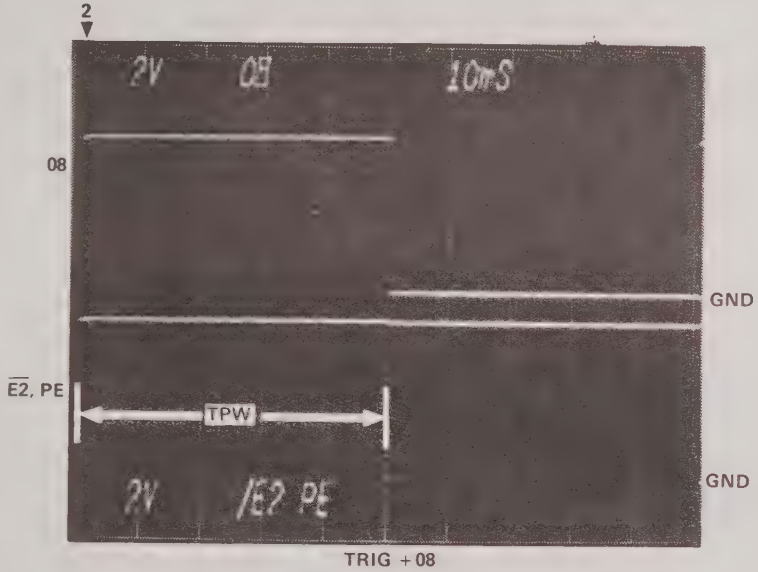
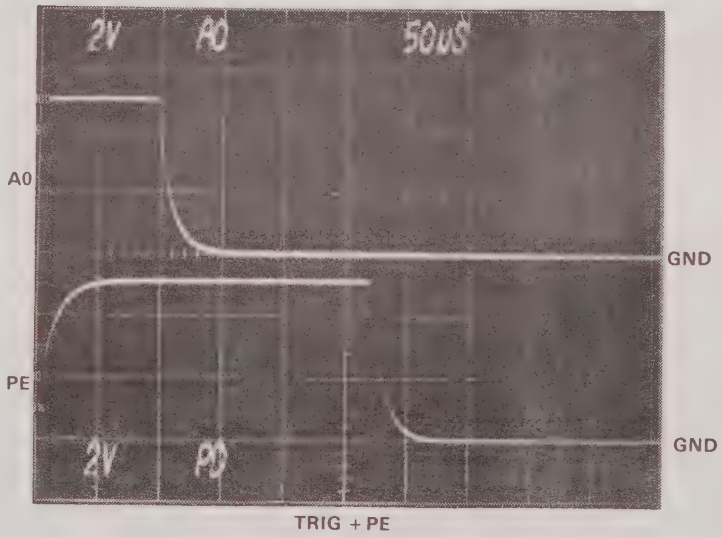


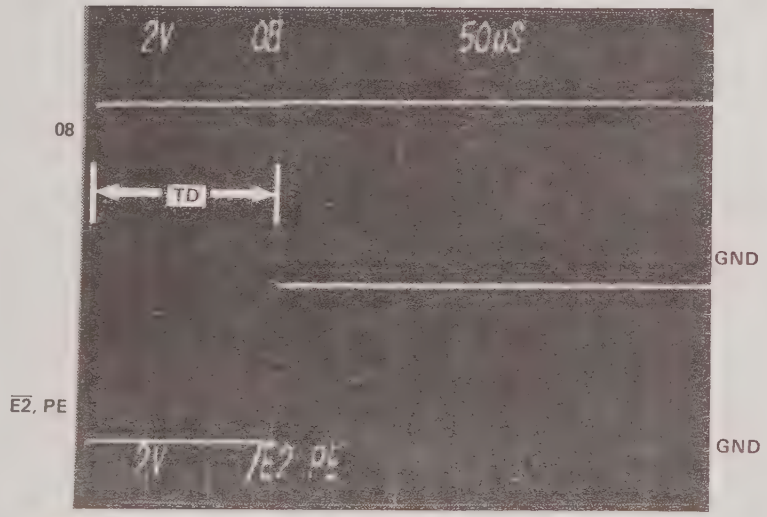
Figure 5-5. Pin names by Device Pinout Numbers, and Socket Configuration by Pinout Code

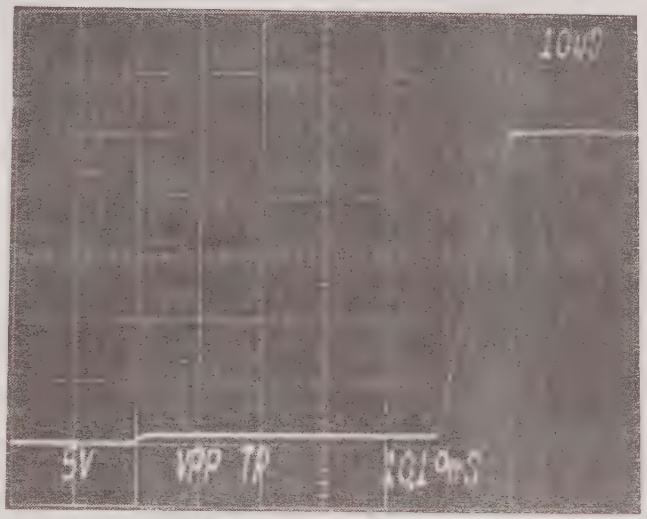

2
2V 08 10mS
08
GND
E2, PE
TPW
GND
2V /E2 PE
TRIG + 08

1


2V A0 50uS
A0
GND
PE
GND
2V PE
TRIG + PE

3


2V 08 50uS
08
TD
GND
E2, PE
GND
2V /E2 PE
TRIG + 08


10uS
5V VPP TR 0.1 mS
VPP TR

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VPP	24	25	26	V	
VPPV	4.75	5.0	5.25	V	
TPW	48	50	52	ms	
TD	2	–	–	µs	
TR	.05	–	–	µs	
TF	.05	–	–	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BZ	8/19/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 19

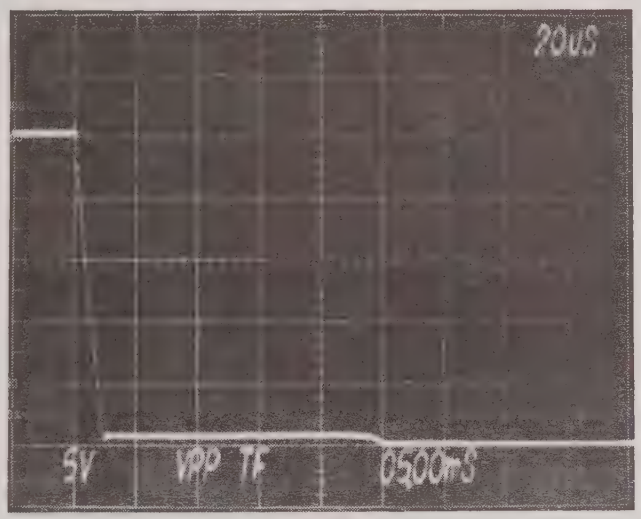
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

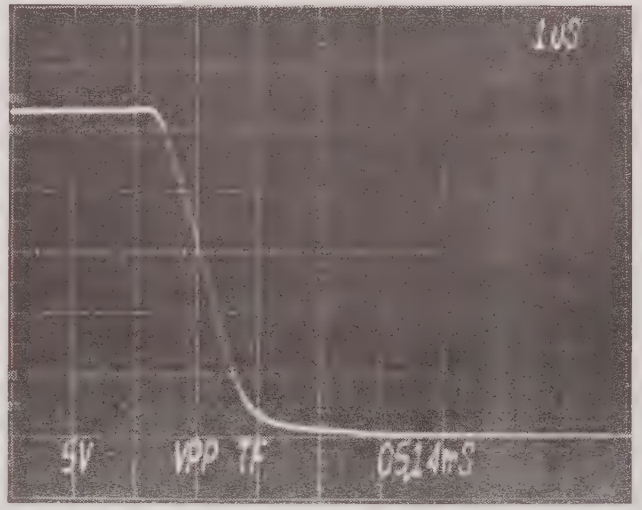
SCALE

SHEET 1/2



VPP TF

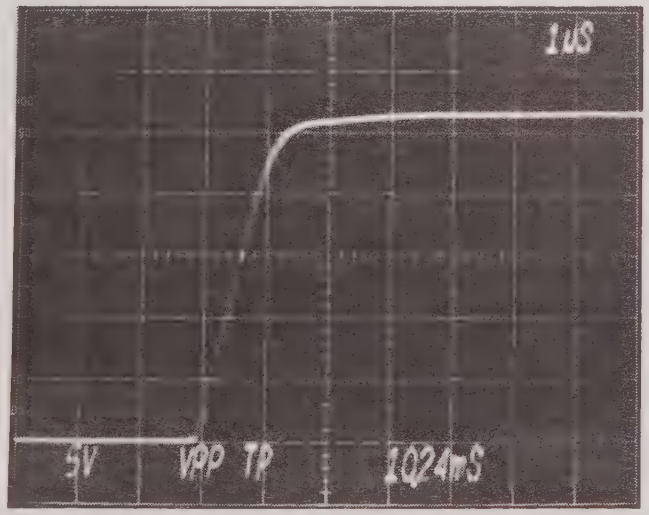
5



VPP TF

7

(Pinout 24)



VPP TR

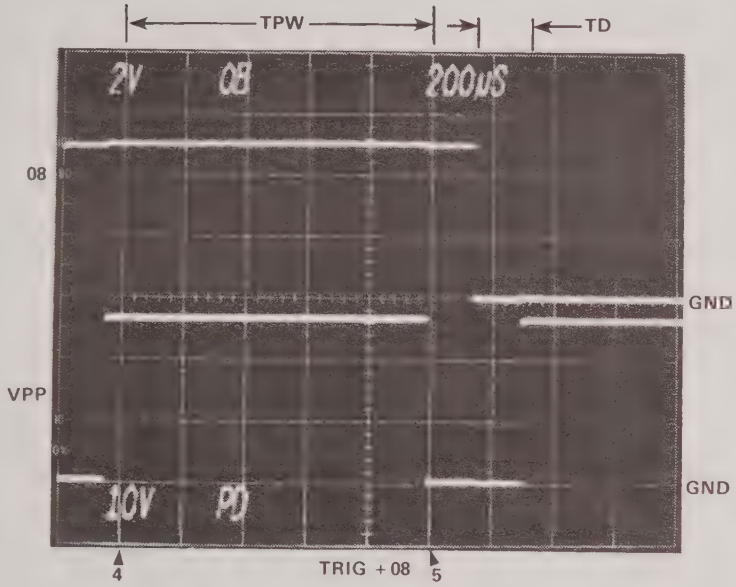
6

(Pinout 24)

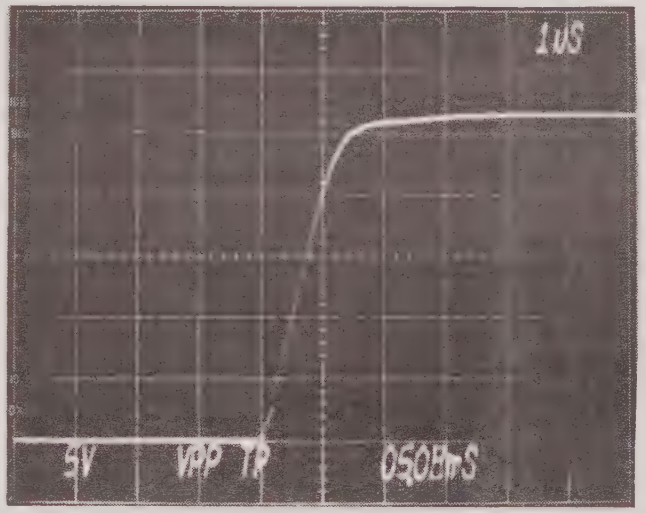
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 19		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 2/2

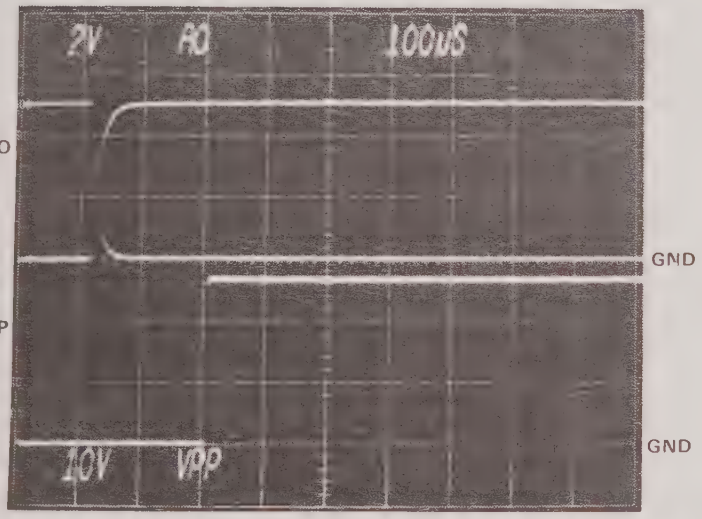


1



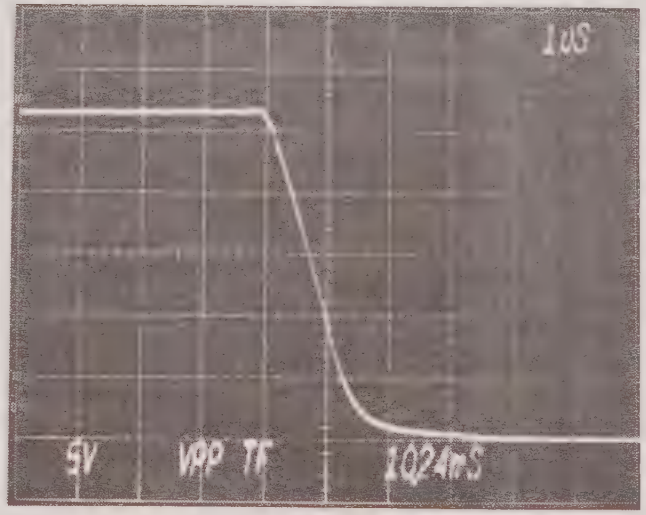
VPP TR

3



TRIG -VPP

2



VPP TF

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VBB	-5.25	-5.0	-4.75	V	Not Shown
VDD	11.4	12.0	12.6	V	Not Shown
VPP	25.0	26.0	27.0	V	
TPW	.8	1.0	1.2	ms	
TR	.5	1.0	1.0	µs	
TF	.5	1.0	2.0	µs	
TD	10		-	µs	
REJECT		100		LOOPS*	*Loop is defined as complete pass from address 0 to max device address appling 1 pulse at each address.
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BL	8/19/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 21

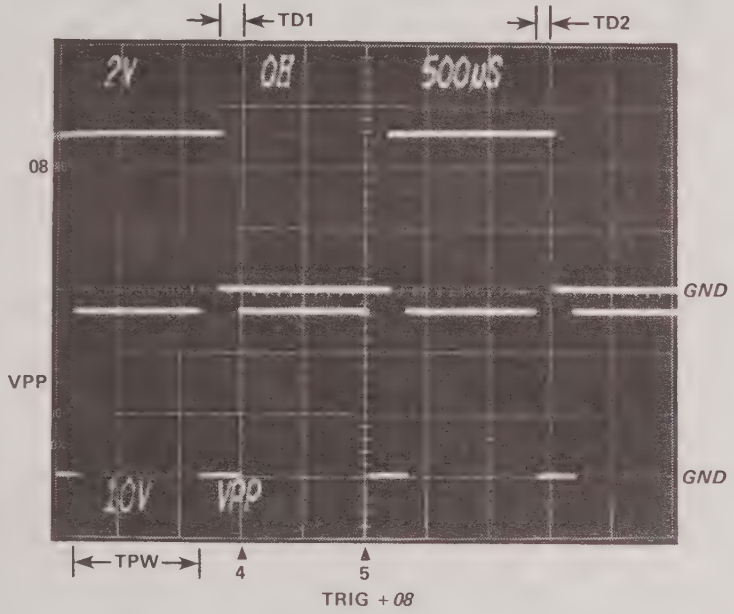
DRAWN BY:

CHECKED BY:

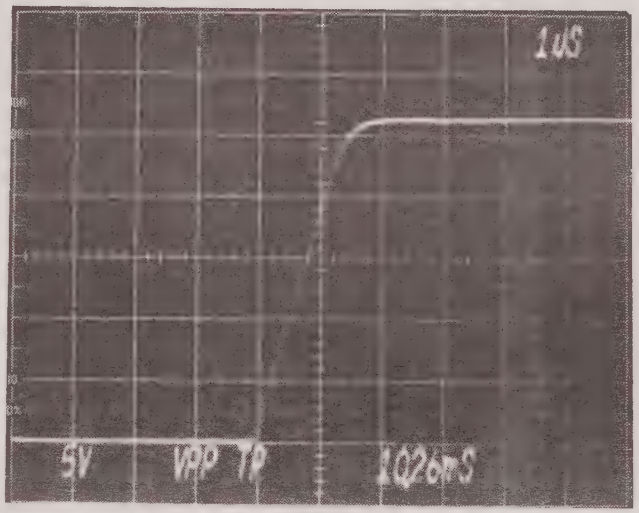
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

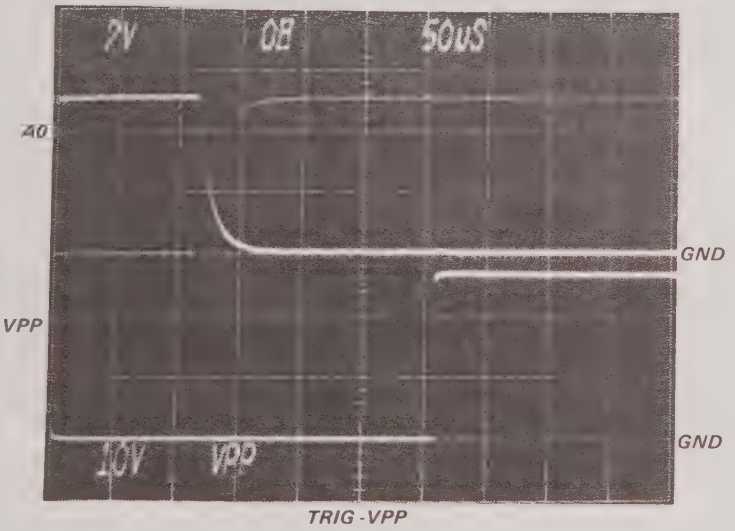
SHEET 1/1


TD1
TD2
2V
0E
500uS
08
GND
VPP
GND
10V
VPP
TPW
4
5
TRIG + 08

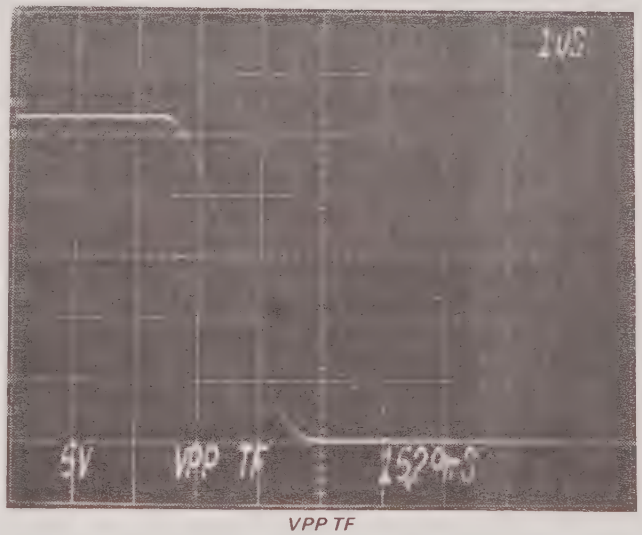
1


1uS
5V
VPP TR
102nS
VPP TR

3


2V
0E
50uS
40
GND
VPP
GND
10V
VPP
TRIG -VPP

2


1uS
5V
VPP TF
152nS
VPP TF

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	11.4	12.0	12.6	V	
VBB	-5.25	5.0	4.75	V	Not Shown
VDD	11.4	12.0	12.6	V	Not Shown
VPP	25.0	26.0	27.0	V	
TPW	.8	1	1.2	ms	
TR	.5	1.0	2.0	µs	
TF	.5	1.0	2.0	µs	
TD1	10	–	–	µs	
TD2	1	–	–	µs	
REJECT		100		LOOPS*	*Loop is defined as complete pass from address 0 to max device address appling 1 pulse at each address.
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BL	8/9/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 23

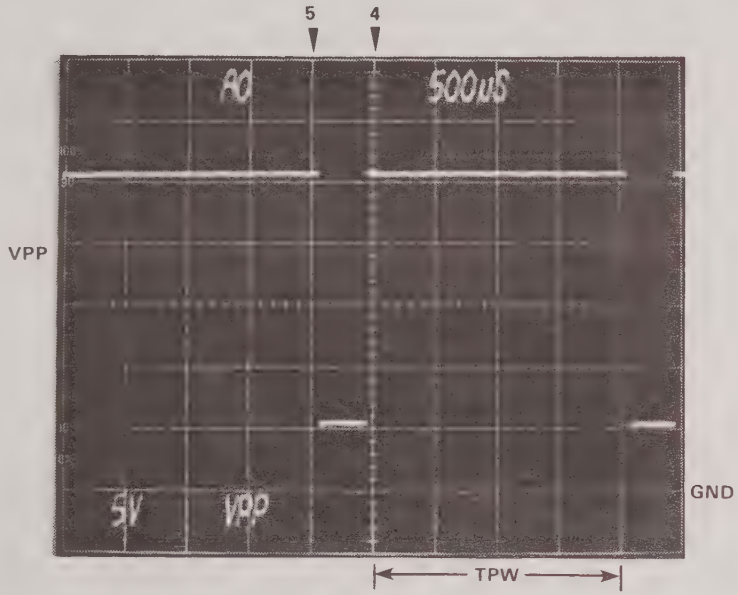
DRAWN BY:

CHECKED BY:

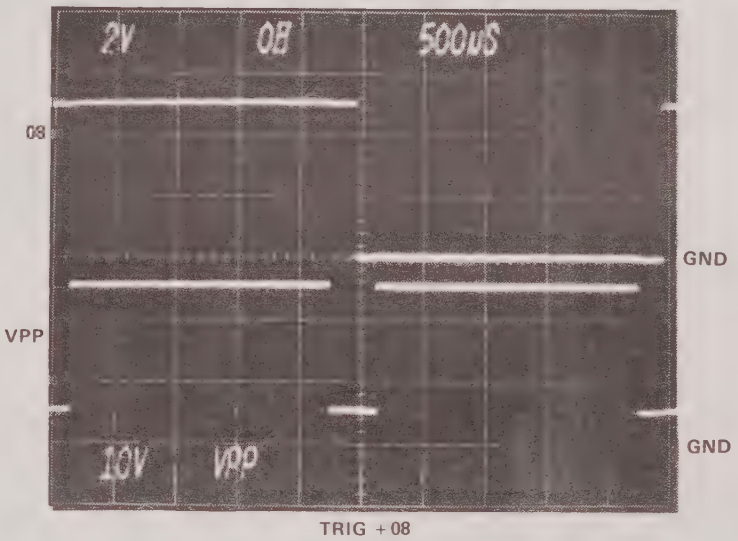
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

SHEET 1/1

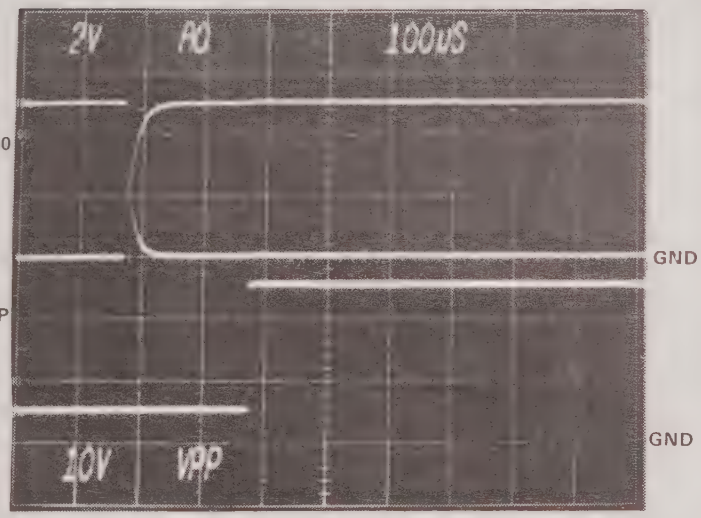


1



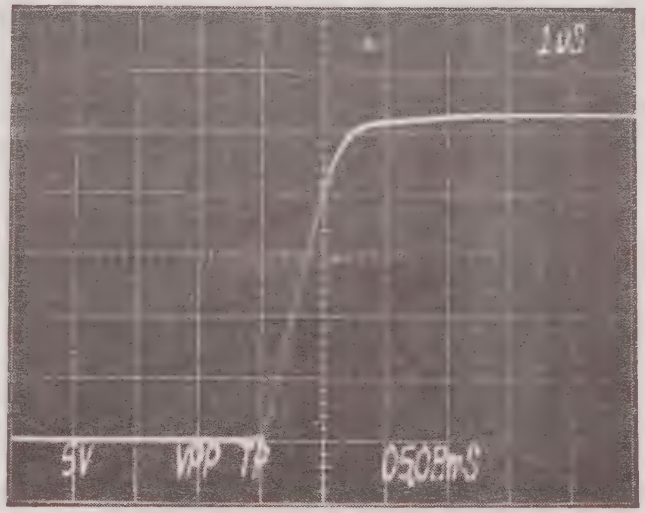
TRIG +08

3



TRIG -VPP

2



VPP TR

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VPP	24	25	26	V	
VPPV	4.6	5.0	5.4	V	
TPW	1.8	2.0	2.2	ms	
TR	0.5	1.0	2.0	µs	
TF	0.5	1.0	5.0	µs	
REJECT		20		PULSES	
OVERPROGRAM		5		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BL	8/19/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 25

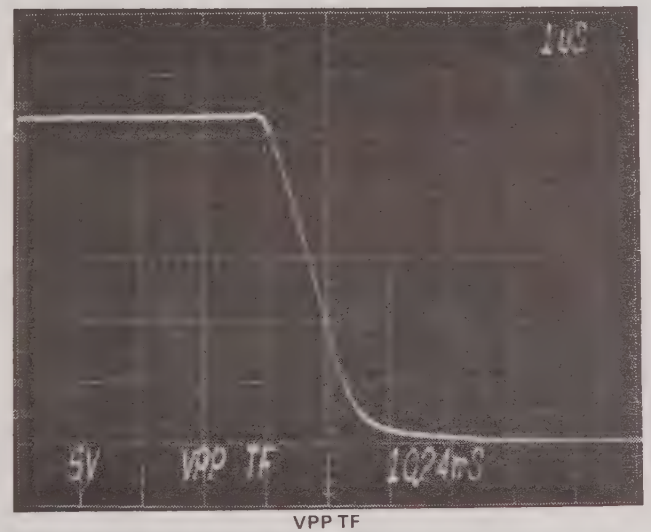
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

SHEET 1/2



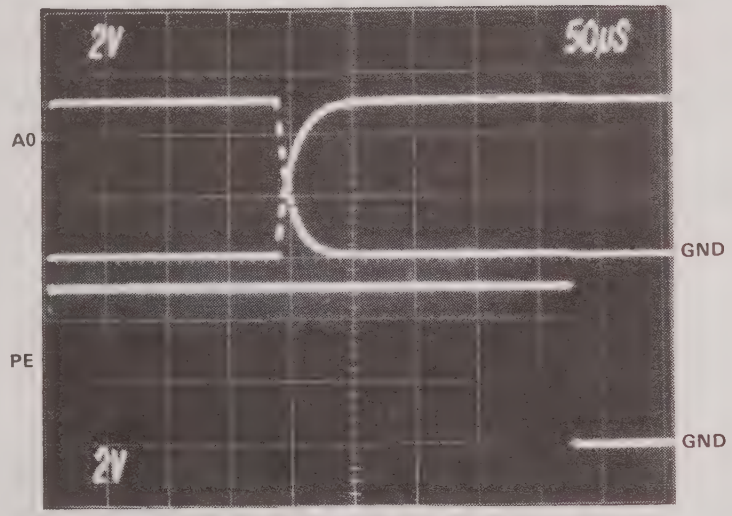
VPP TF

5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

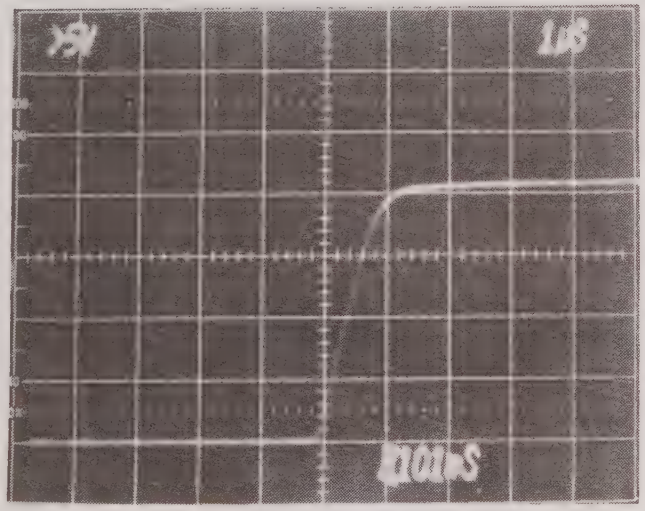
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 25		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 2/2



TRIG + PE

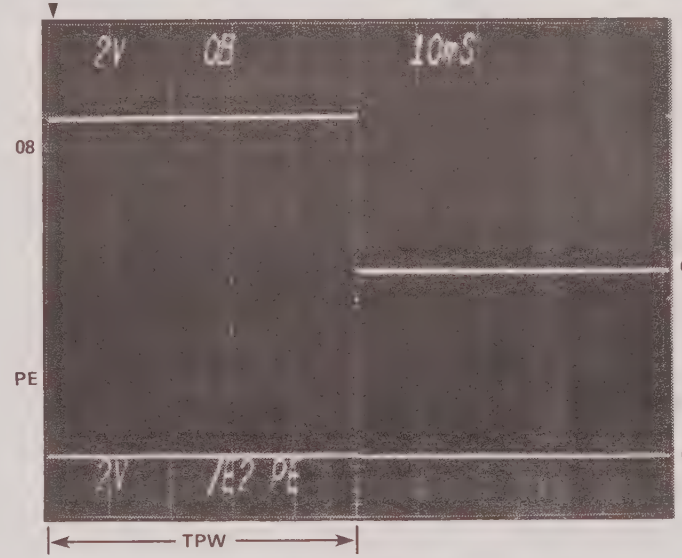
1



VPP TR

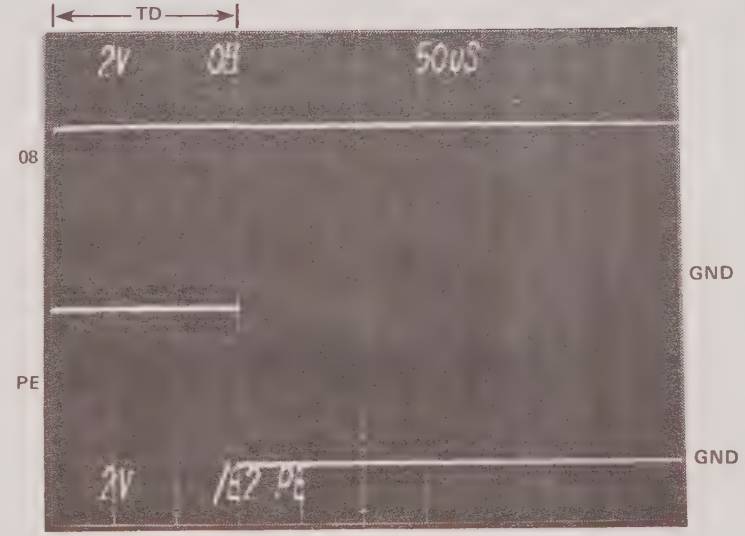
2

4



TRIG + 08

3



TRIG + 08

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.00	5.25	V	Not Shown
VPP	20.5	21.0	21.5	V	
TD	2	–	–	μs	
TPW	48	50	52	ms	
TR	50	–	–	ns	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		B L	8/19/82

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 27

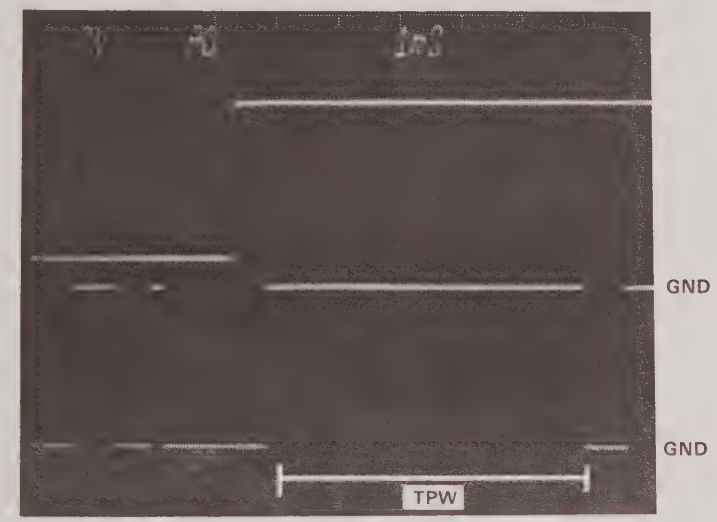
DRAWN BY:

CHECKED BY:

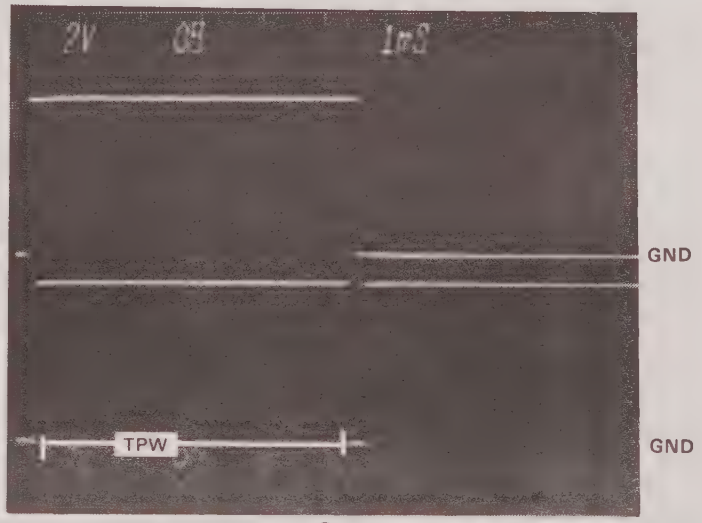
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

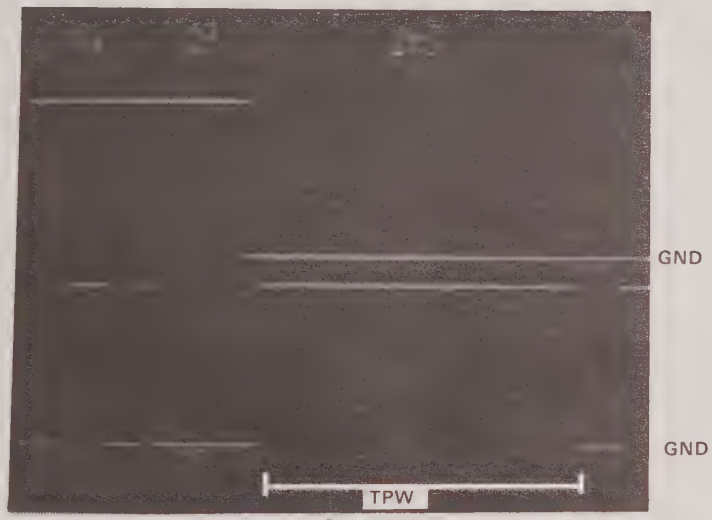
SHEET 1/1



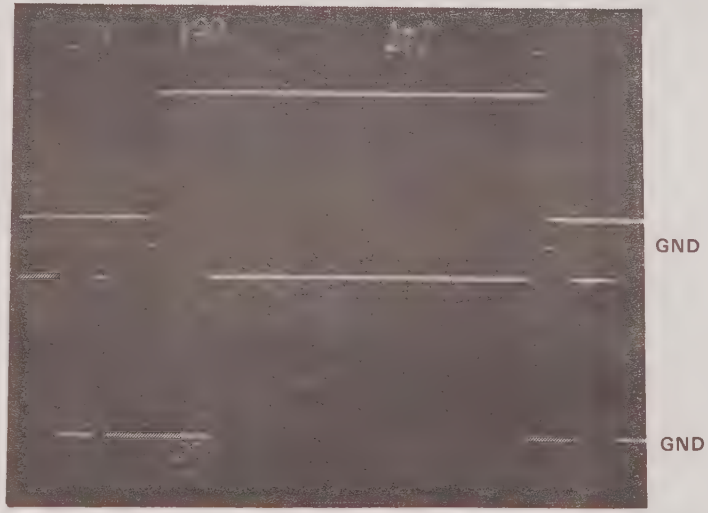
1
(PINOUT 23)



3
(PINOUT 23 - OVERPROGRAM)



2
(PINOUT 23)



TRIG + PE
4
(PINOUT 23)

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *► with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VPP	24	25	26	V	
VPR	4.75	5	5.25	V	
TPW	4.9	5.0	5.1	ms	
TD	2			µs	
Reject		5		PULSES	
Overprogram	1		5	PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			
	B	ECN #4678		BL	10/28/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

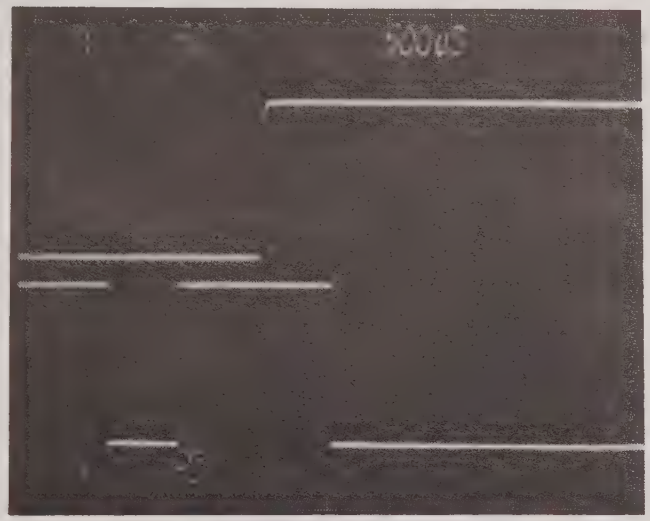
FAMILY CODES 31

DRAWN BY: BL

CHECKED BY: DC

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

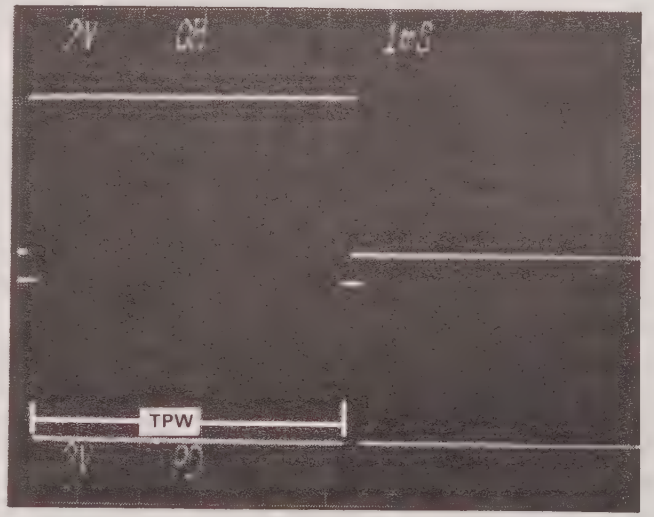
SCALE | SHEET 1/3



TRIG + PE

5

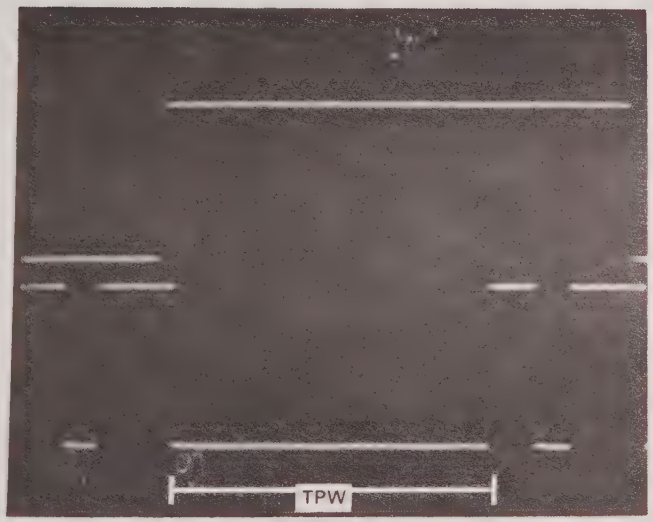
(PINOUTS 25 & 30)



TRIG + PE

7

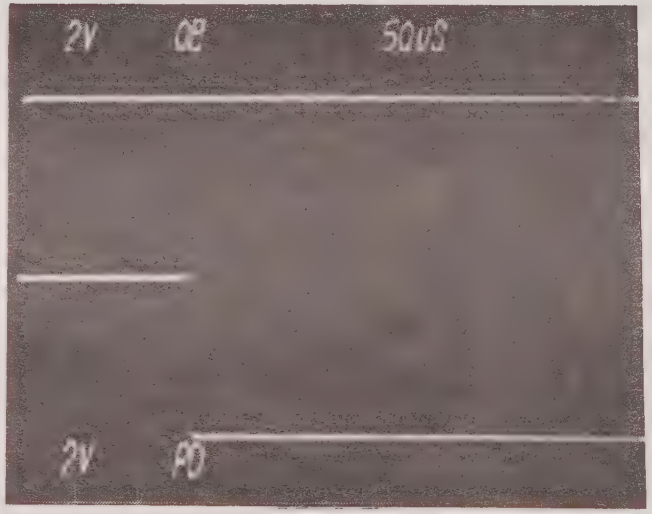
(PINOUTS 25 & 30 OVERPROGRAM)



TRIG + PE

6

(PINOUTS 25 & 30)



TRIG + 08

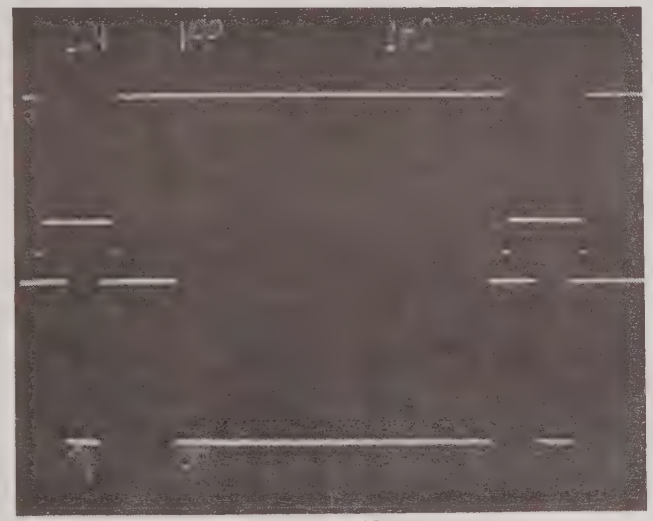
8

(PINOUTS 25 & 30)

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

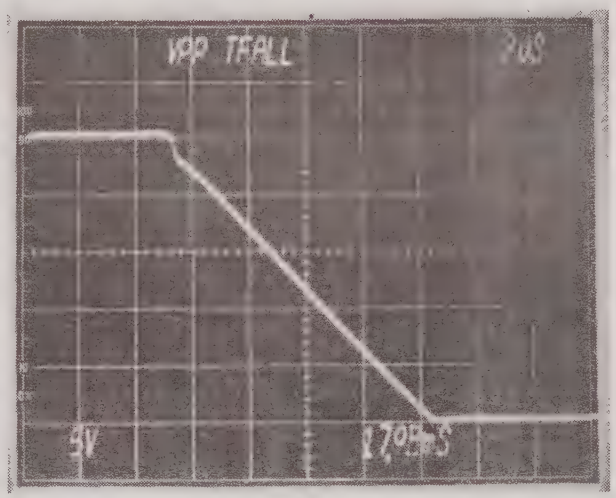
TITLE: TIMING DIAGRAM FAMILY CODES 31			DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120	
SCALE			SHEET 2/3



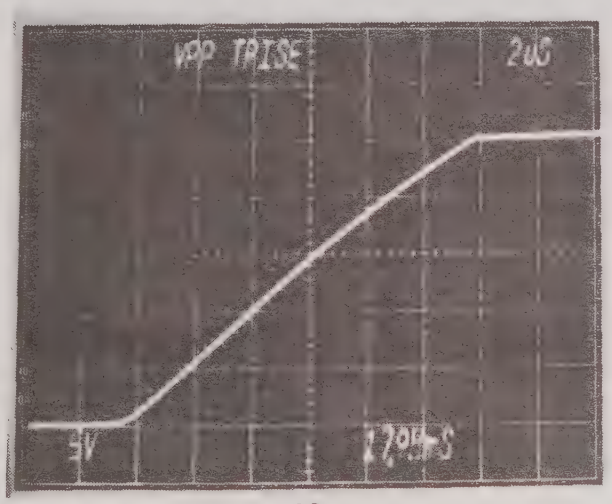
TRIG + PE

9

(PINOUTS 25 & 30)



11

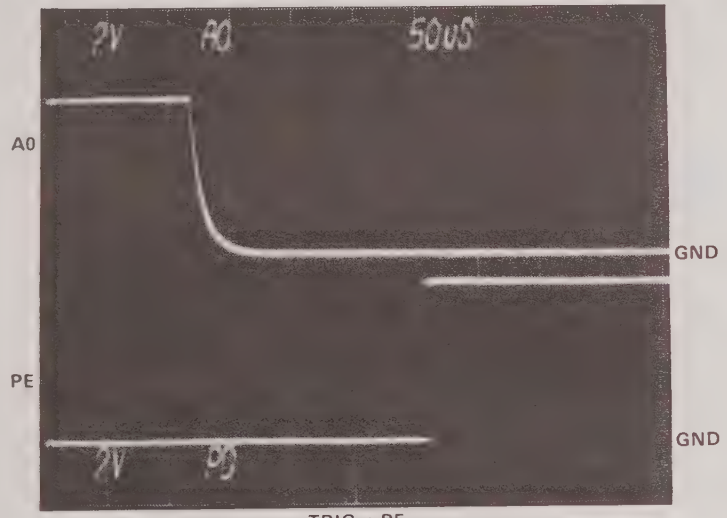


10

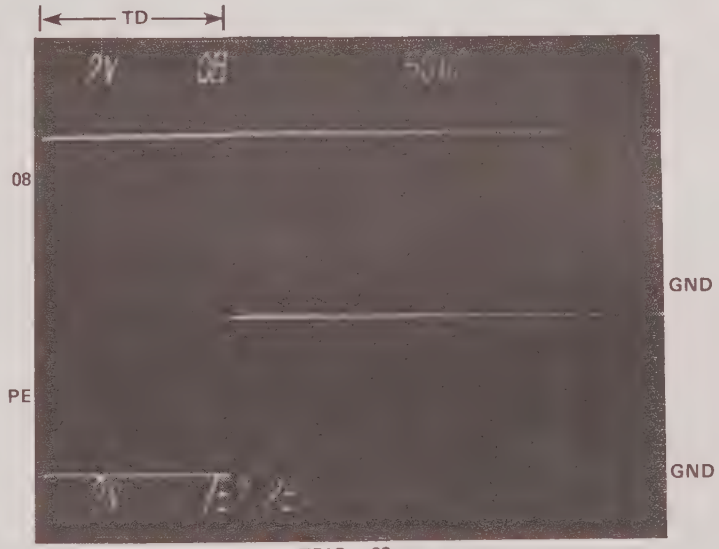
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

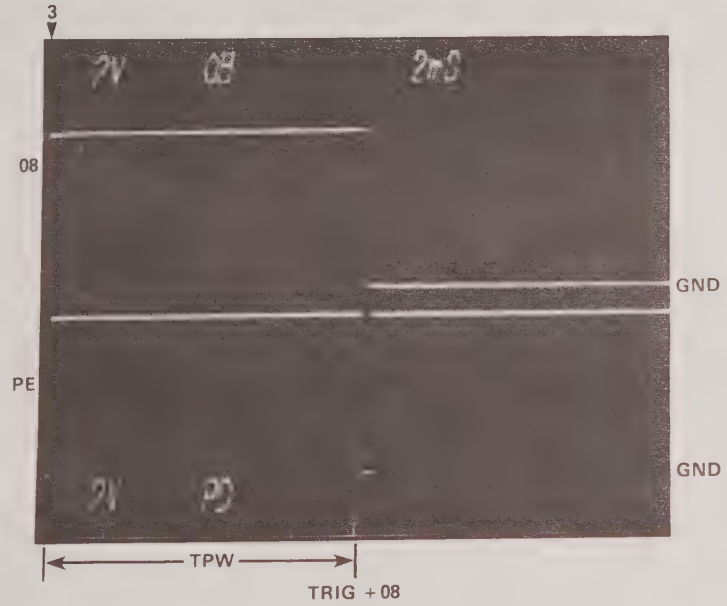
TITLE: TIMING DIAGRAM FAMILY CODES 31		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 3/3


A0
GND
PE
GND
TRIG + PE

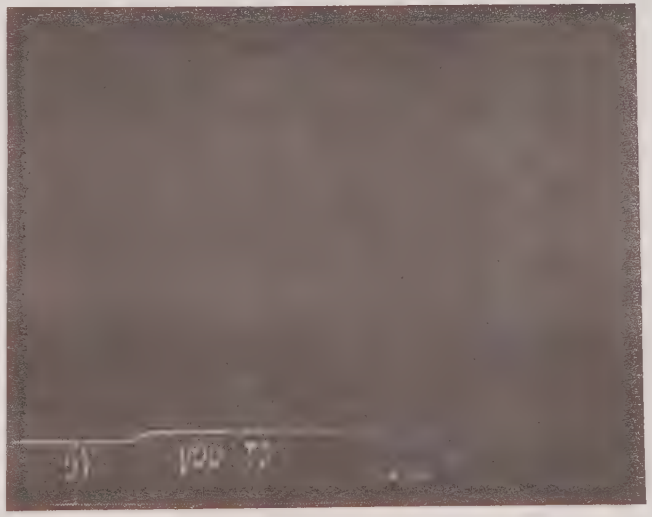
1


TD
08
GND
PE
GND
TRIG + 08

3


3
08
GND
PE
GND
TPW
TRIG + 08

2


VPP TR

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VPP	24	25	26	V	
VPPV	4.75	5.0	5.25	V	
TPW	9.8	10.0	10.2	ms	
TD	2			µs	
TR	.05	—	—	µs	
TF	.05	—	—	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BL	8/14/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 33

DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

SHEET 1/2

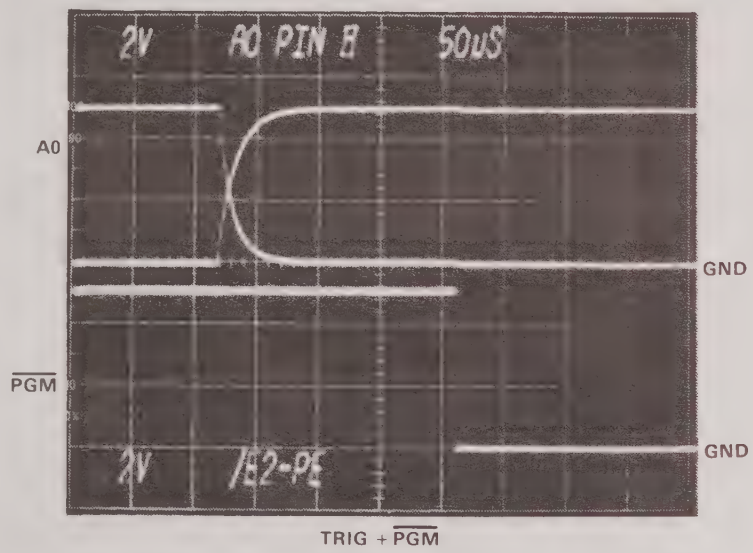
VPP TF

5

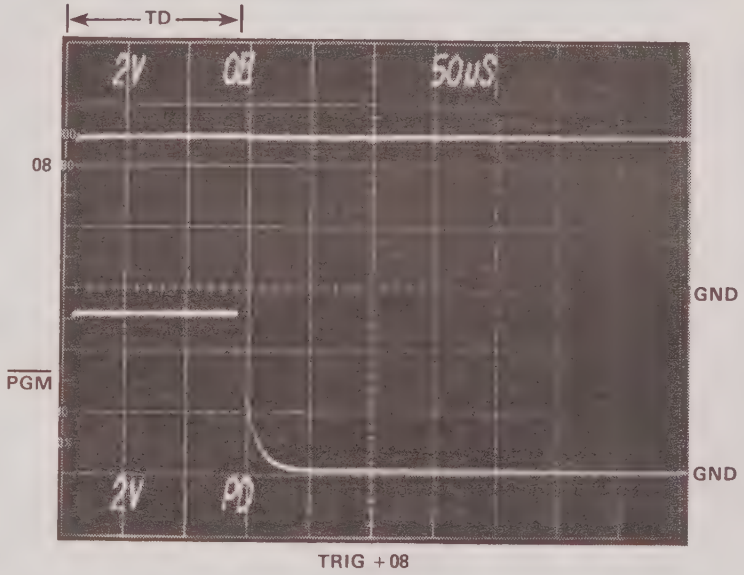
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

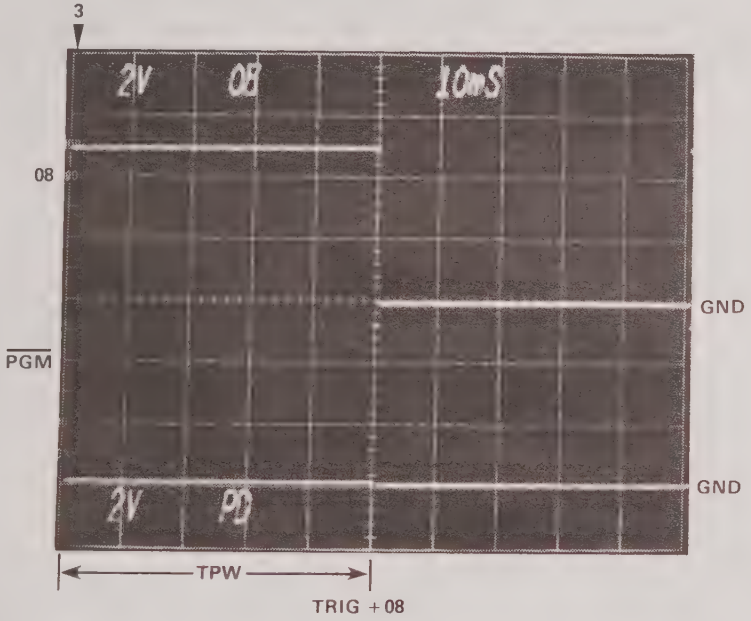
TITLE: TIMING DIAGRAM FAMILY CODES 33		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 2/2

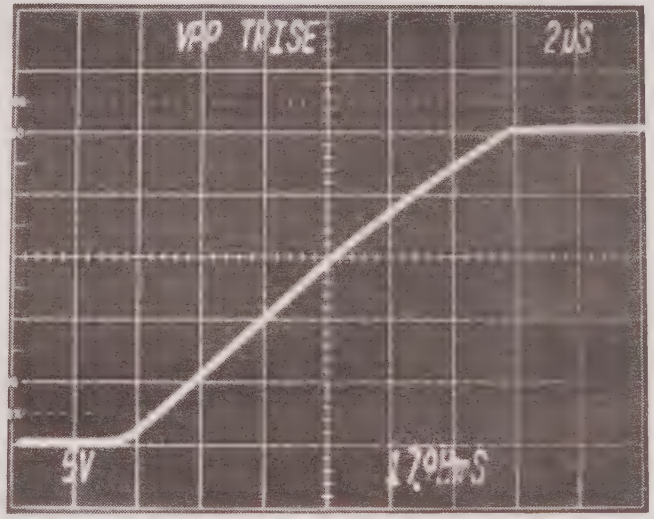

2V A0 PIN B 50uS
A0
GND
PGM
GND
2V
TRIG + PGM

1


TD
2V 08 50uS
08
GND
PGM
GND
2V PD
TRIG + 08

3


3
2V 08 10mS
08
GND
PGM
GND
2V PD
TPW
TRIG + 08


VPP RISE 2uS
5V

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.00	5.25	V	Not Shown
VPP	20.5	21.0	21.5	V	
TD	2	—	—	µs	
TPW	48	50	52	ms	
TR	50	—	—	ns	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BZ	8/19/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 35

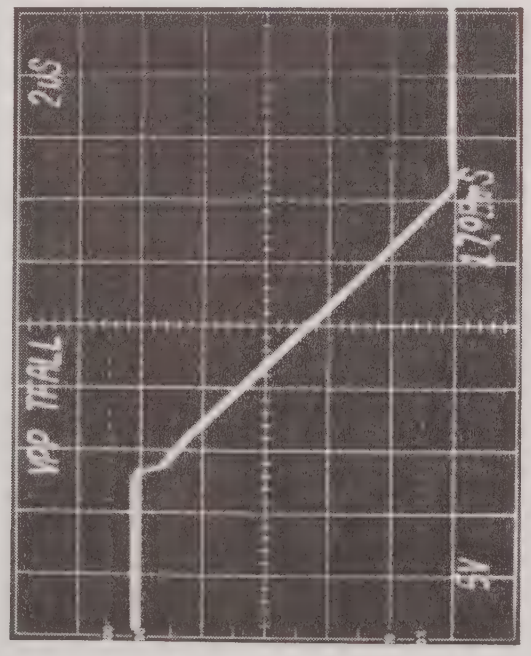
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

SHEET 1/2

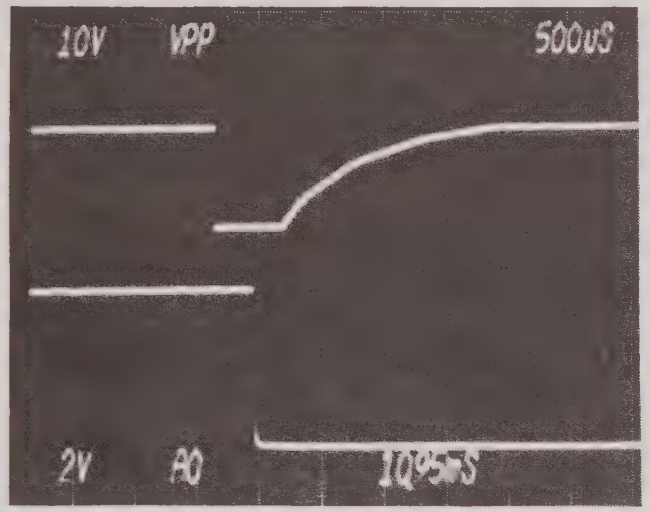


5

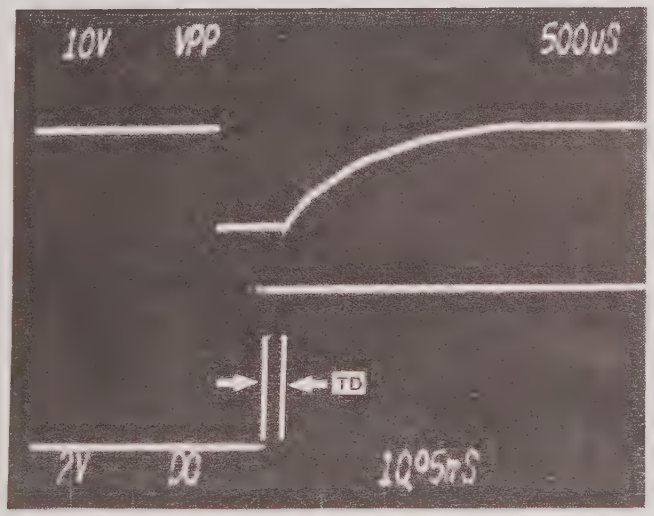
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 35		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 2/2



1



2

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.00	5.25	V	Not Shown
VPP	20	21.0	22	V	
TD	2	—	—	μs	
TPW	48	50	52	ms	
TR	450	600	750	μs	RC time constant
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BZ	3/19/82

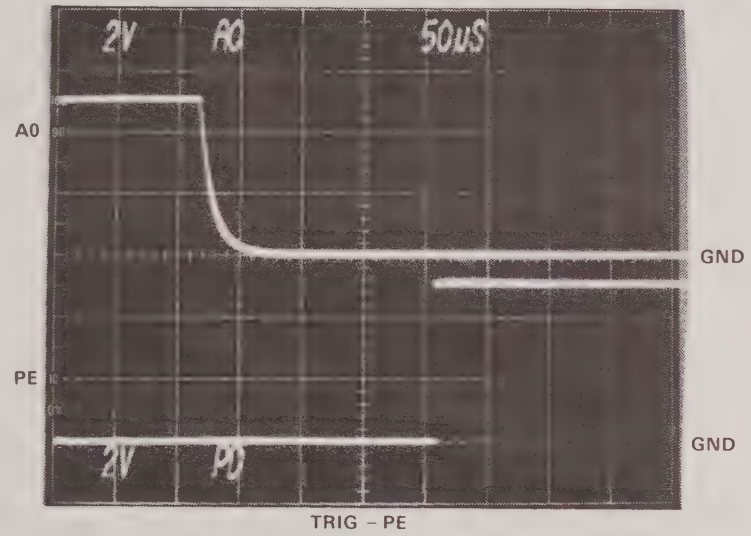
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM
FAMILY CODES 37

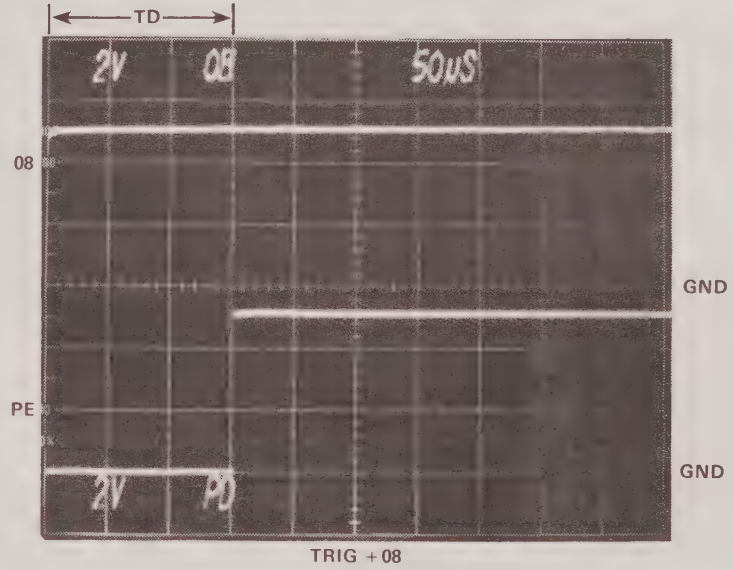
DRAWN BY:
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

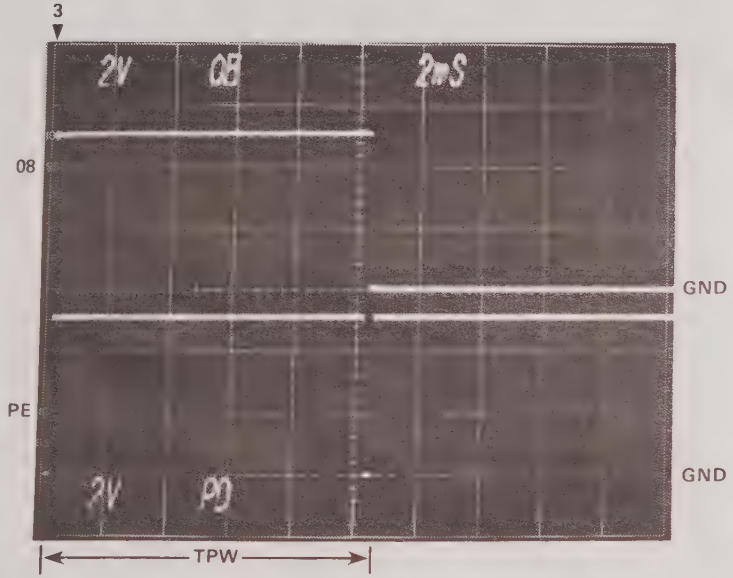
SCALE | SHEET 1/1


2V A0 50uS
A0
GND
PE
GND
2V PD
TRIG – PE

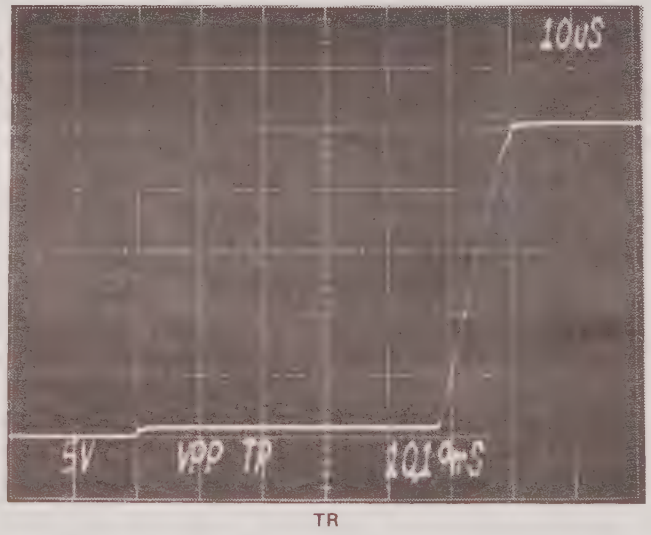
1


TD
2V Q8 50uS
Q8
GND
PE
GND
2V PD
TRIG + Q8

3


3
2V Q8 2mS
Q8
GND
PE
GND
2V PD
TPW

2


10uS
5V VPP TR 1Q1 9mS
TR

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VPP	24	25	26	V	
VPPV	4.75	5.0	5.25	V	
TPW	9.8	10.0	10.2	ms	
TD	2			µs	
TR	.05	—	—	µs	
TF	.05	—	—	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		BZ	8/19/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 43

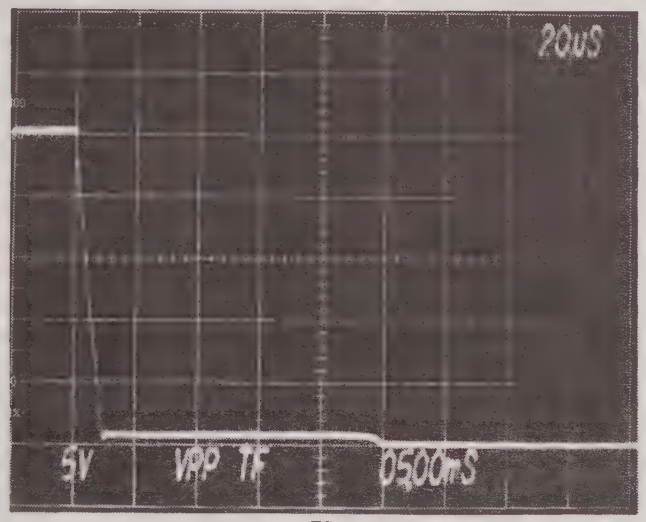
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

SHEET 1/2



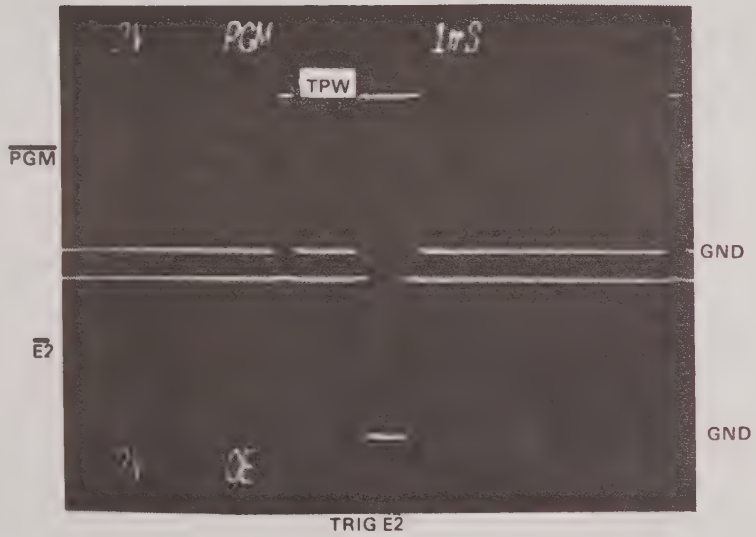
TF

5

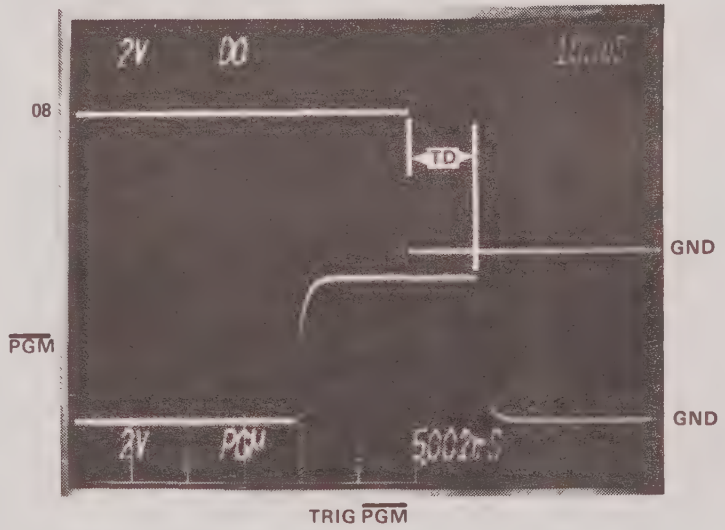
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 43		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 2/2

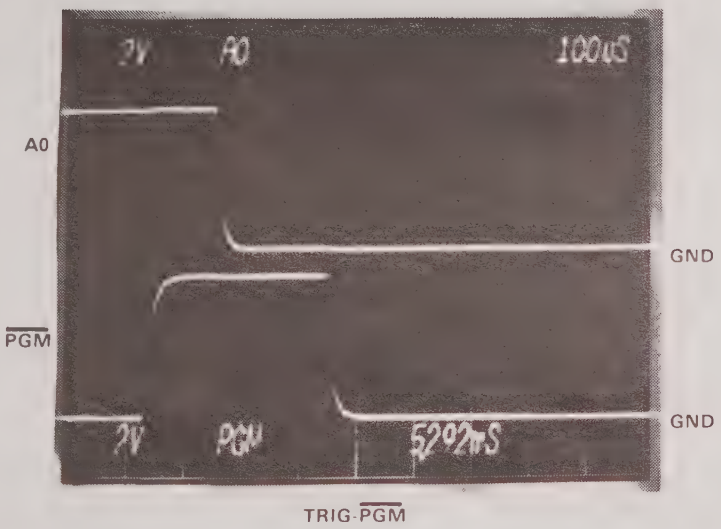


1

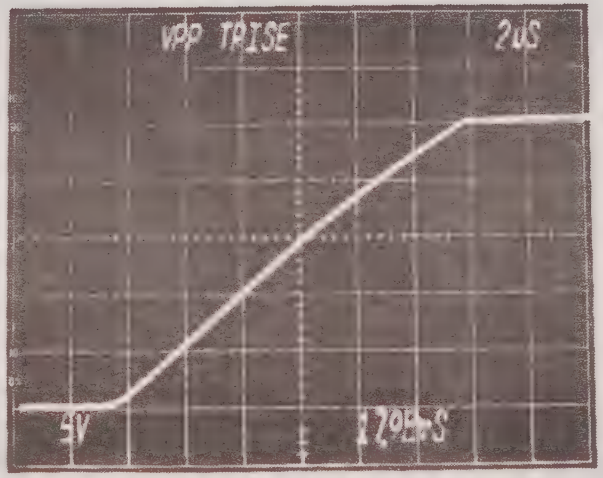


3

2764 Fast 79 33



2



4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	5.75	6.00	6.25	V	Not Shown
VPP	20.5	21.0	21.5	V	
TD	2	—	—	μs	
TPW	.9	1	1.1	ms	
TR	50	—	—	ns	
REJECT		15		PULSES	
OVERPROGRAM		1		PULSE	Pulse width is equal to 4 msec times the number of pulses applied to any address for first verify.

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4678		BL	10/28/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 79

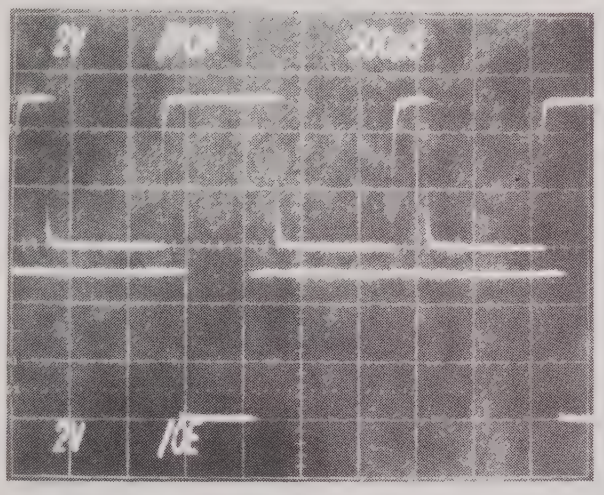
DRAWN BY: BG.

CHECKED BY: D.C.

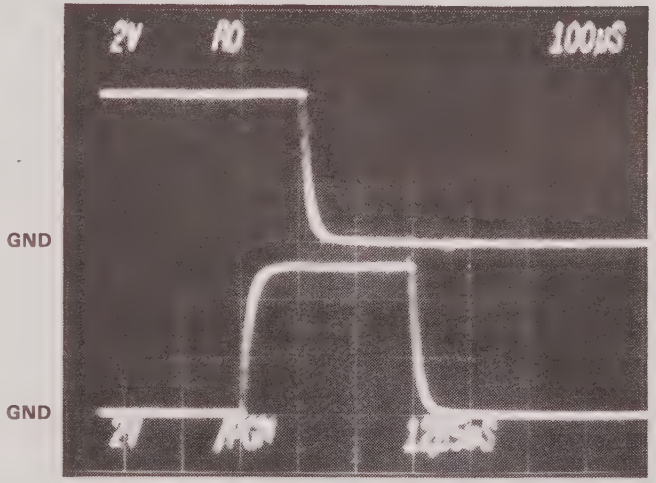
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

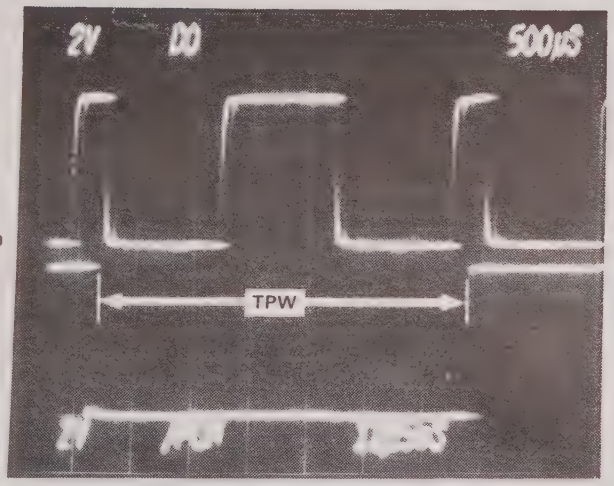
SHEET 1/2



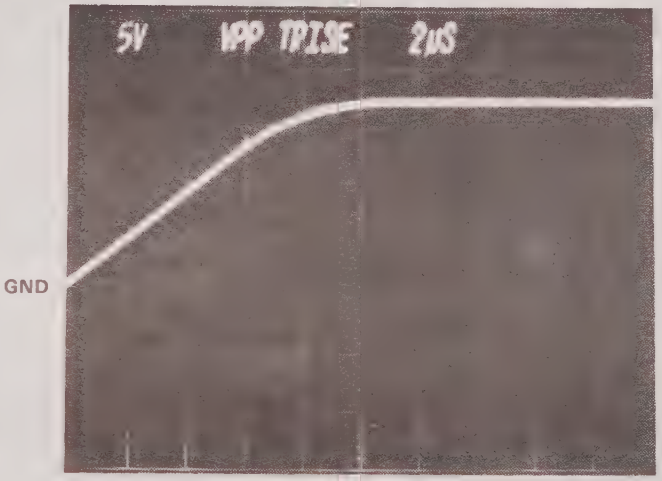
1



2



3



4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
	VCCP	5.75	6.0	6.25	V	Not Shown
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	0.9	1.0	1.1	ms	
	TD	2	-	-	µs	
	TR	50	-	-	ns	
	REJECT		20		PULSES	
	OVERPROGRAM		1		PULSES	Pulse width is equal to 1 msec times the number of pulses applied to any address for first verify.

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN# 4978		MJS	10-28-83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE 45

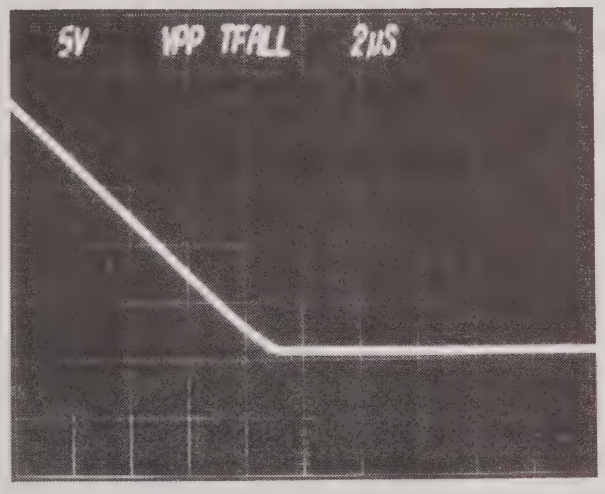
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2



5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN# 4978		MDS	10-28-85

DATA I/O

TITLE

TIMING DIAGRAM
FAMILY CODE 45

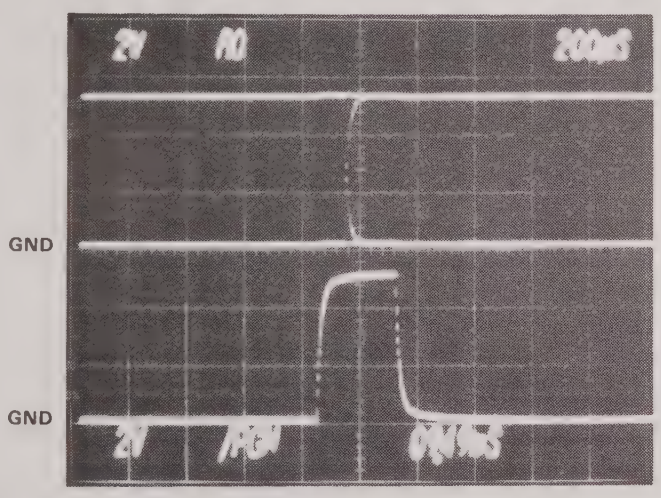
DRAWN BY:

CHECKED BY:

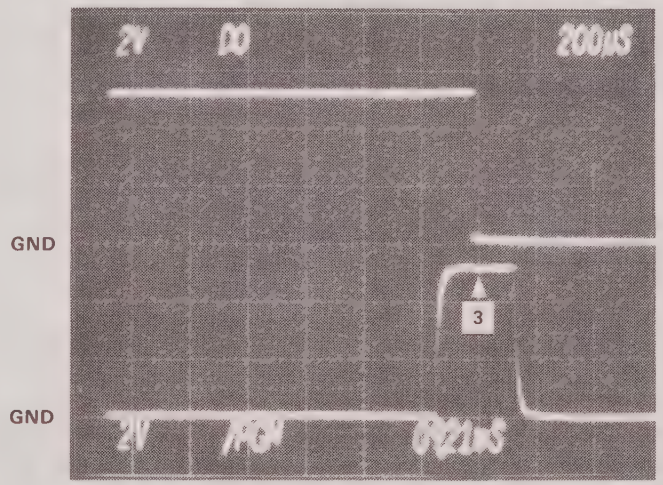
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

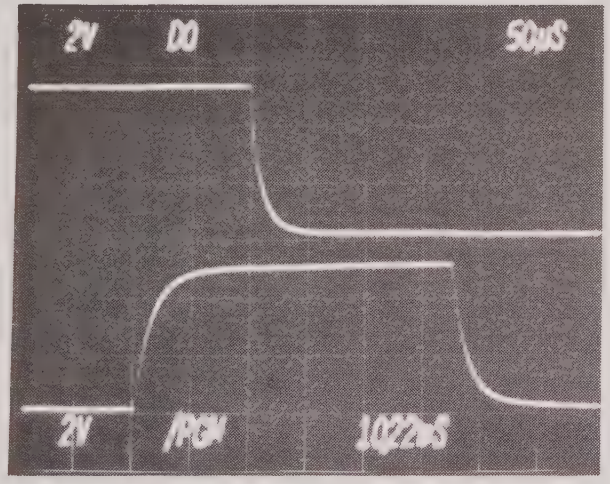
SHEET 2/2


2V
200μS
GND
GND
2V

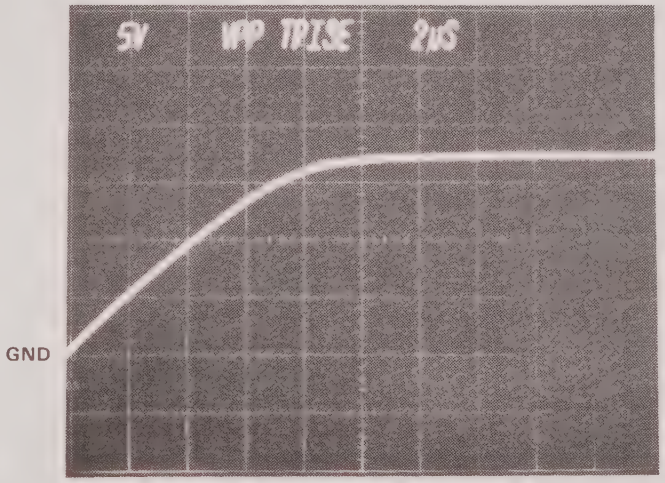
1


2V
200μS
GND
3
GND
2V

2


2V
50μS
GND
GND
2V

3


5V
2μS
GND

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	20.5	21.0	21.5	V	
	TPW	9.0	10	11	ms	
	TD	2	-	-	ms	
	TR	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		M.U.S.	10-28-83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE 63

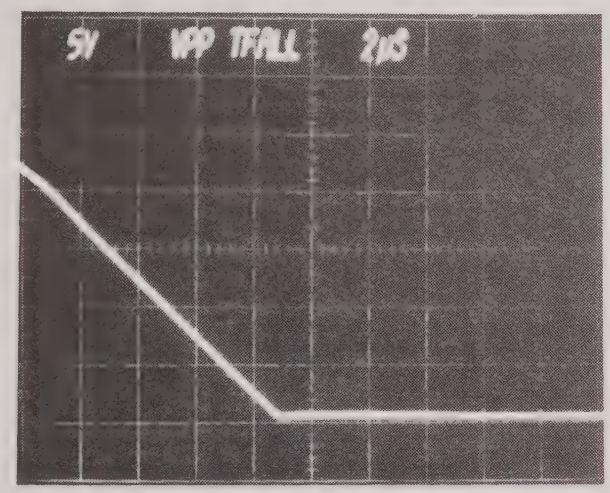
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2

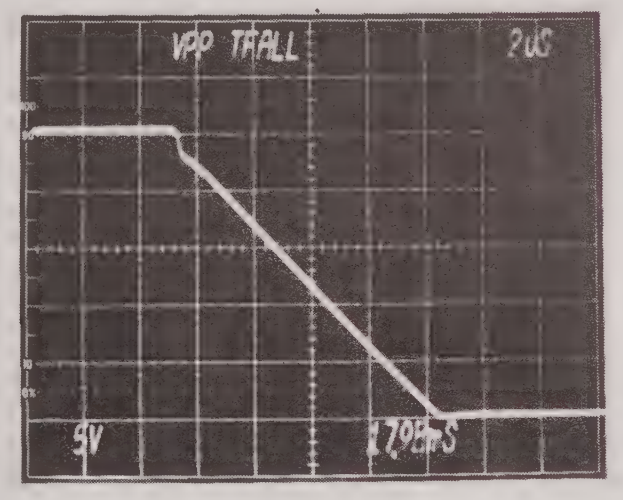


5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		mjd. S	10-24-83

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODE 63		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.
SCALE		SHEET 2/2

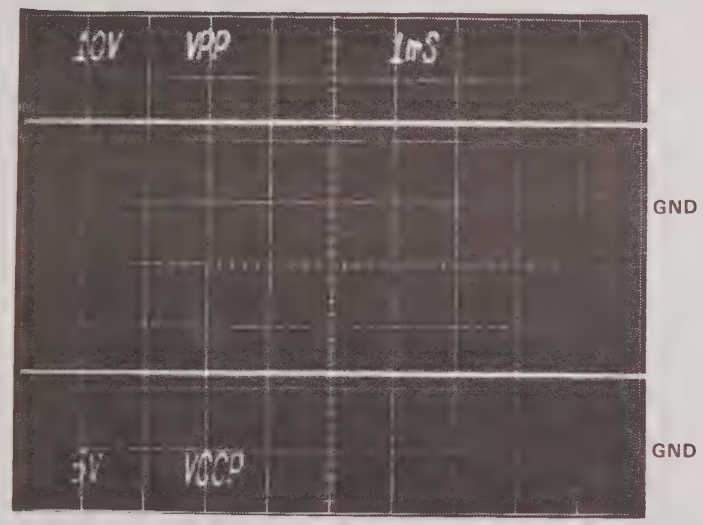


5

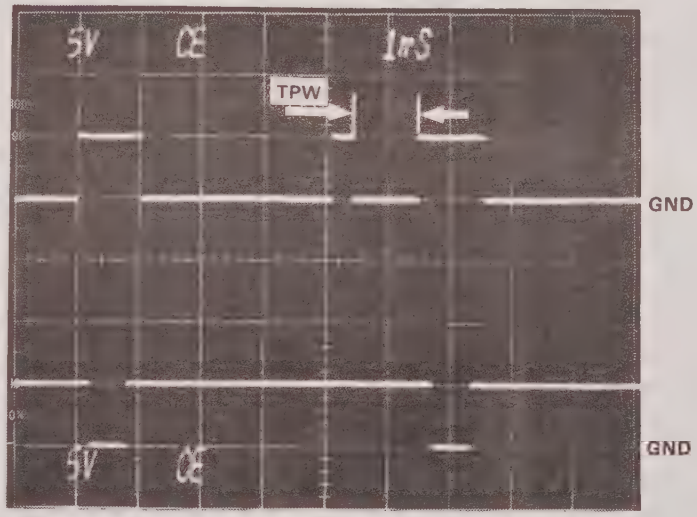
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

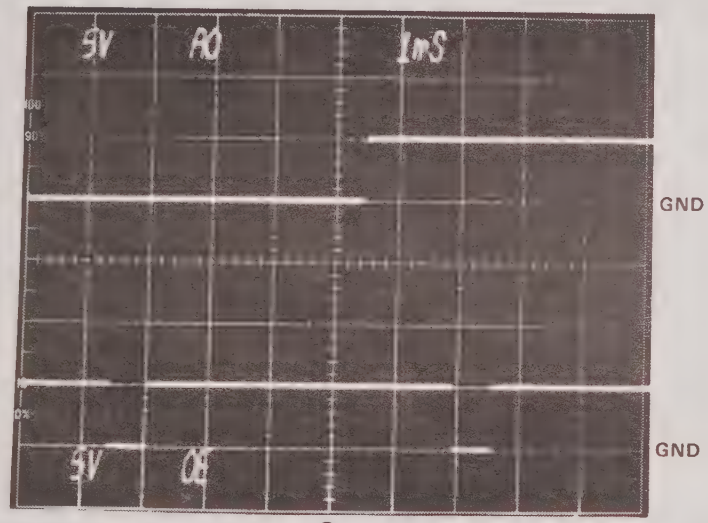
TITLE: TIMING DIAGRAM FAMILY CODES 79		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 2/2


10V VPP 1mS
GND
5V VCCP
GND

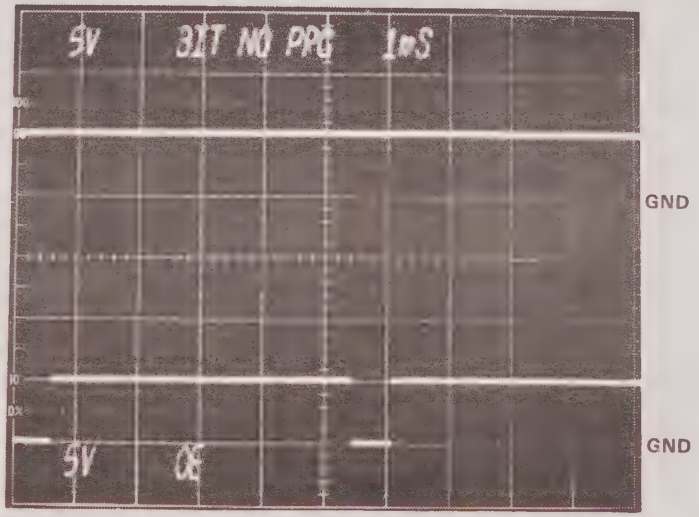
1


5V CE 1mS
TPW
GND
5V CE
GND

2


5V AO 1mS
GND
5V CE
GND

3


5V BIT NO PPC 1mS
GND
5V CE
GND

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout.*
3. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	5.75	6.00	6.25	V	Not Shown
VPP	12.0	12.5	13.0	V	
TD	2	-	-	us	
TPW	.9	1	1.1	ms	
TR	50	-	-	ns	
Reject		25		PULSES	
Overprogram		1		PULSE	Pulse width is equal to 3 msec times the number of pulses applied to any address for first verify.

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4678		DT	5.16

DATA I/O

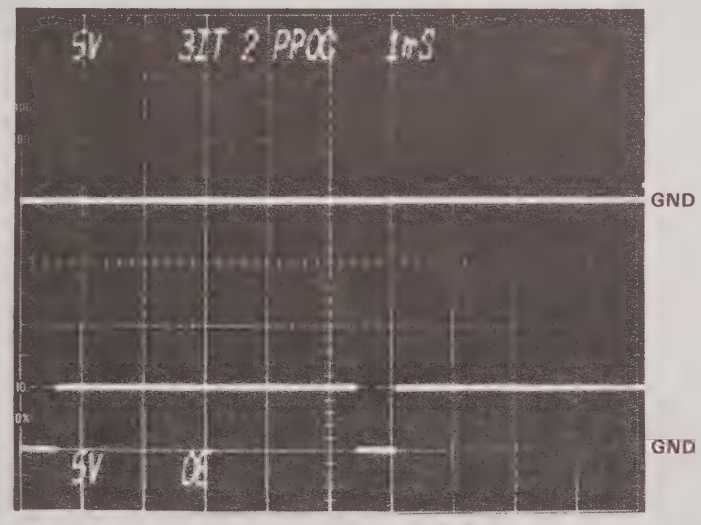
TITLE
TIMING DIAGRAM
FAMILY CODE 93

DRAWN BY: BL
CHECKED BY: D.C.

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0120

SCALE

SHEET 1/2

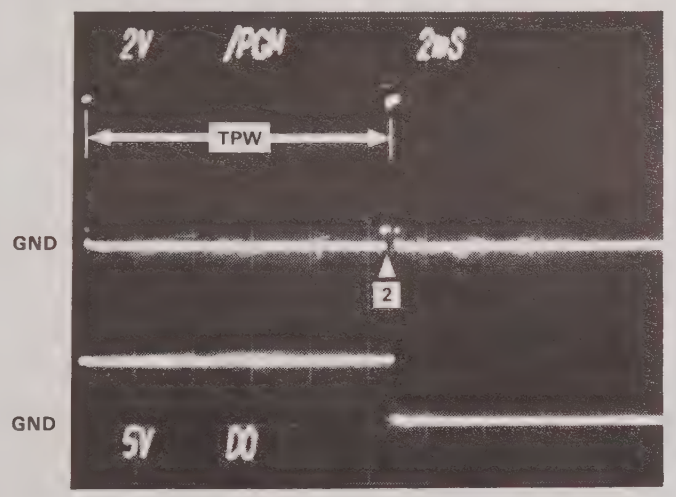


5

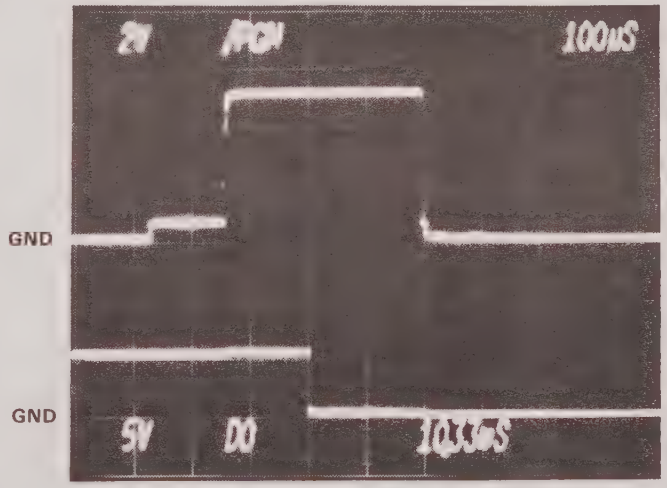
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1			

DATA I/O

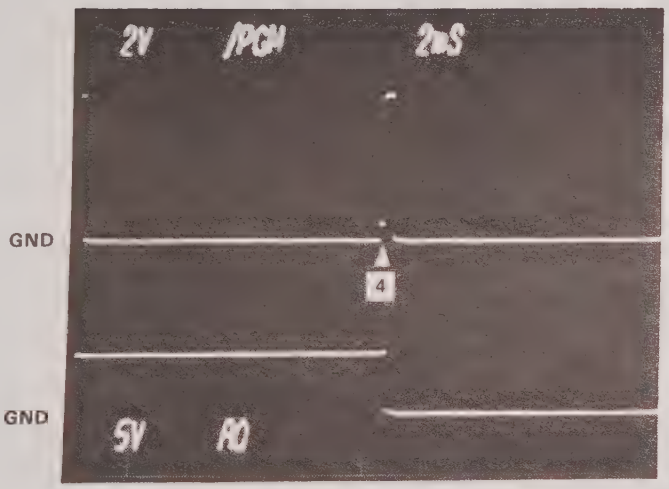
TITLE: TIMING DIAGRAM FAMILY CODE 93		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-990-0120
SCALE		SHEET 2 of 2


2V
/PCH
2mS
TPW
GND
2
GND
5V
DO

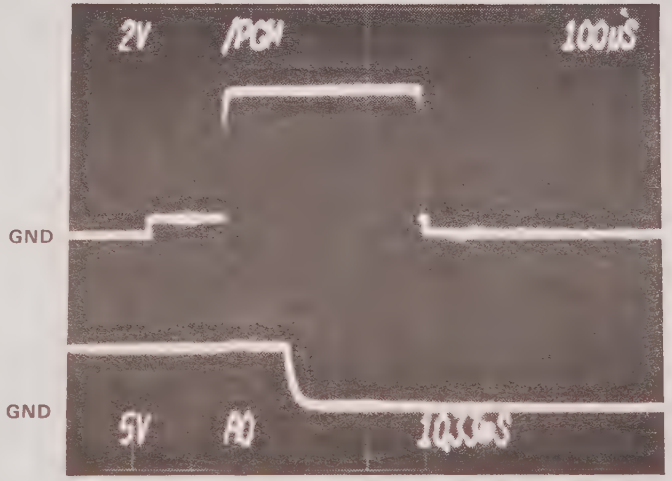
1


2V
/PCH
100uS
GND
GND
5V
DO

2


2V
/PCH
2mS
GND
4
GND
5V
RO

3


2V
/PCH
100uS
GND
GND
5V
RO

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*
7. *Photo 5 is erase waveform.*

WAVEFORM VARIABLES

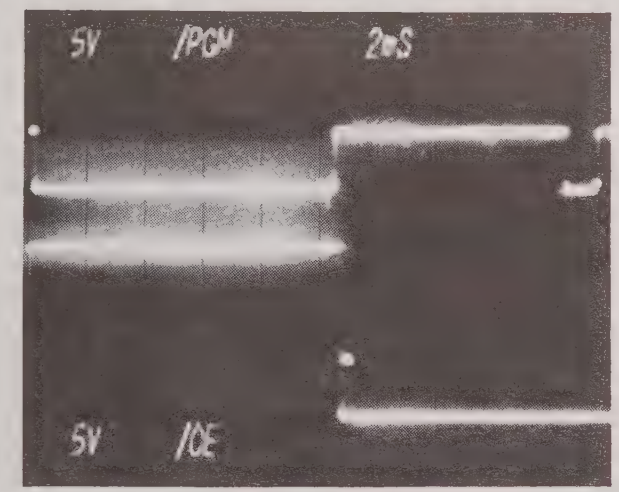
	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.5	5.0	5.5	V	
	VPP	0.0	0.0	0.8	V	
	VEE	12.0	14.5	21.0	V	
	TPW	5.0	10.0	15.0	ms	
	TD	2	-	-	µs	
	TR	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		mjs	10.25-83

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODE A5		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.
SCALE		SHEET 1/2



5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MJS	10-28-83

DATA I/O

TITLE

TIMING DIAGRAM
FAMILY CODE A5

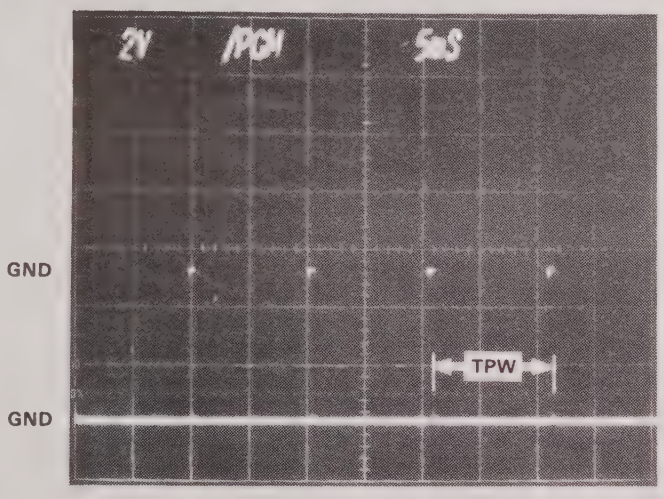
DRAWN BY:

CHECKED BY:

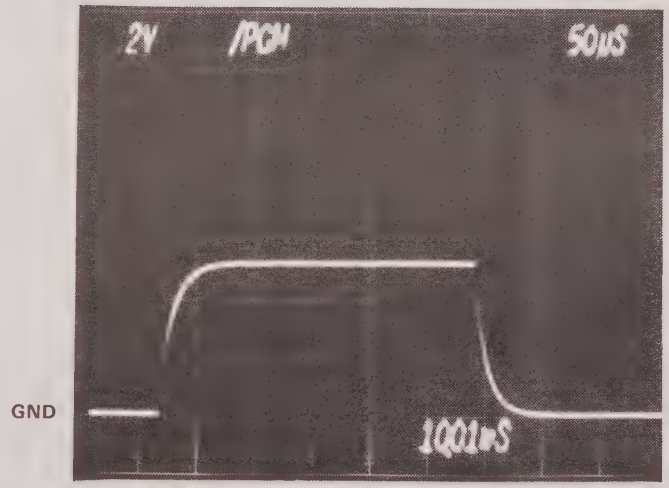
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

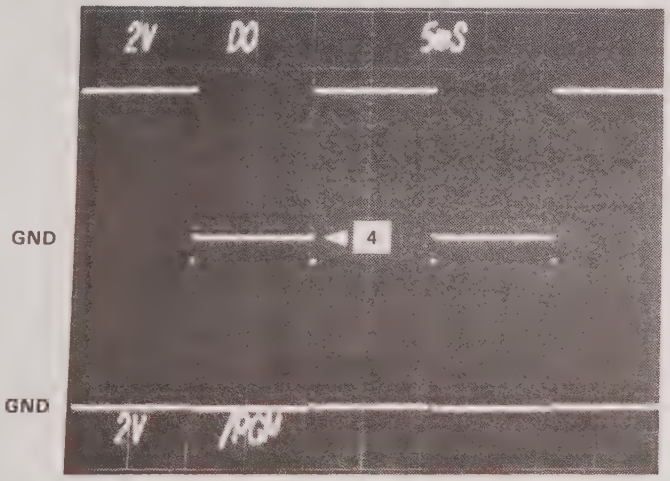
SHEET 2/2


2V
/PCH
5mS
GND
TPW
GND

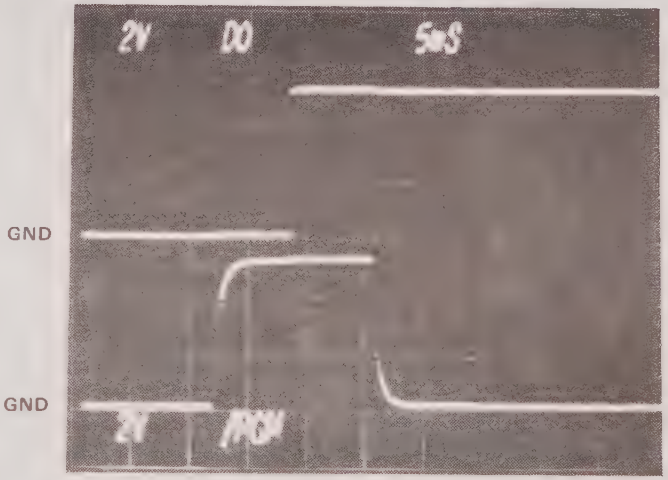
1


2V
/PCH
50µS
GND
100µS

2


2V
DO
5mS
GND
4
GND
2V
/PCH

3


2V
DO
5mS
GND
GND
2V
/PCH

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	4.75	5.0	5.25	V	
	TPW	-	10	-	ms	
	TD	2	-	-	ms	
	TR	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		M.J.S	10-28-87

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE AB

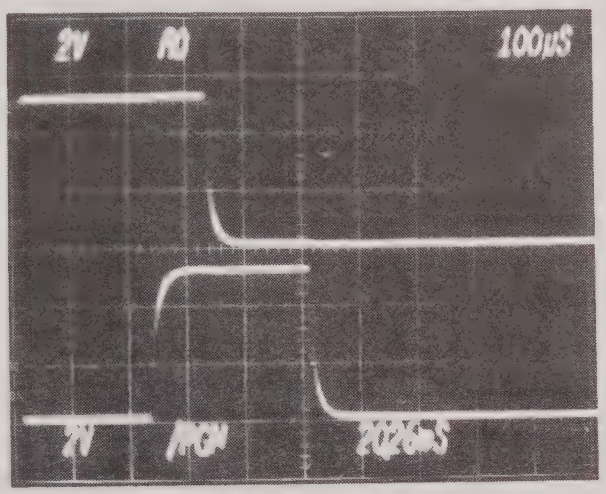
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2

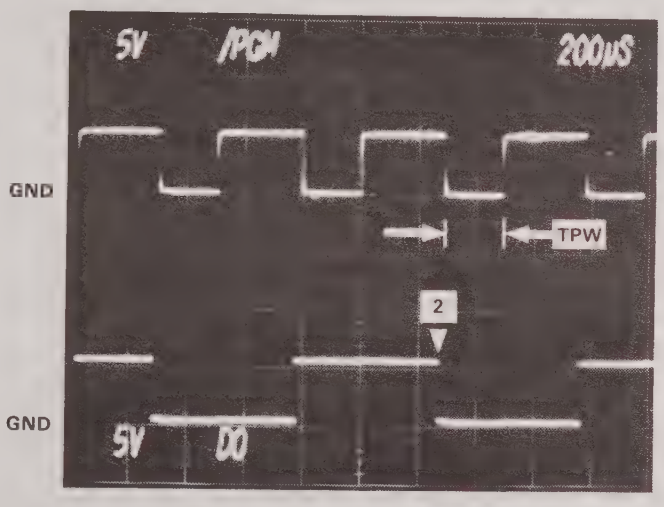


5

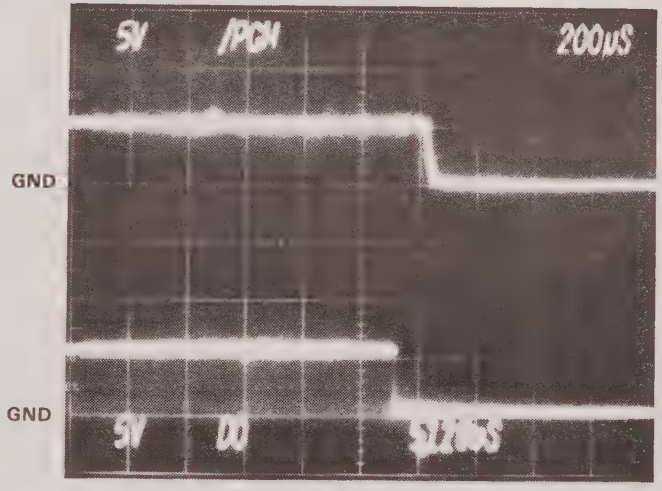
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MVS	10-28-83

DATA I/O

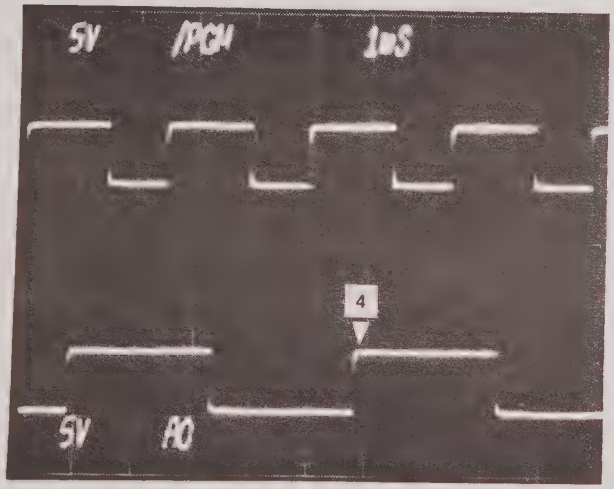
TITLE: TIMING DIAGRAM FAMILY CODE AB		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.
SCALE		SHEET 2/2


5V
/PCH
200uS
GND
TPW
2
GND
5V
DO

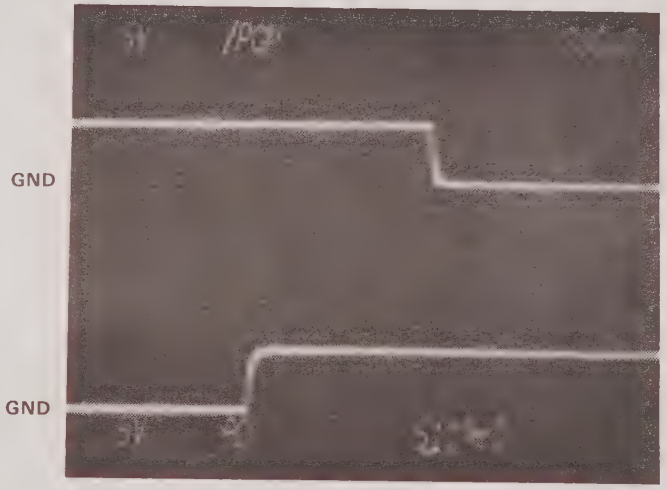
1


5V
/PCH
200uS
GND
GND
5V
DO

2


5V
/PCH
1uS
4
5V
AO

3


GND
GND

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*
7. *Overprogram pulse.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VPP	21.0	21.5	22.0	V	
	TPW	0.95	1.0	1.05	ms	
	REJECT		25		PULSES	
	OVERPROGRAM		1		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MJS	10-28-83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE AF

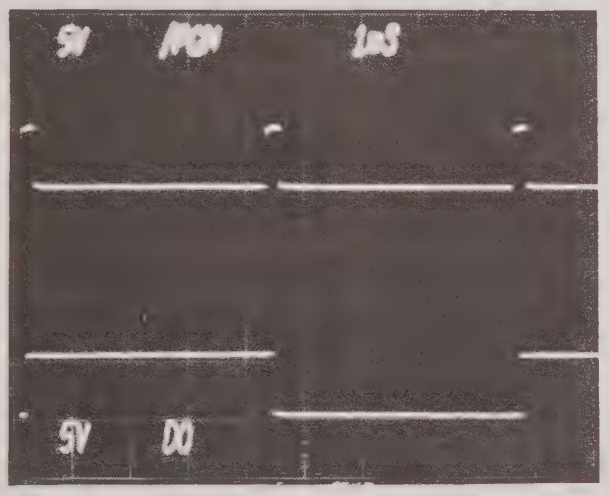
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2

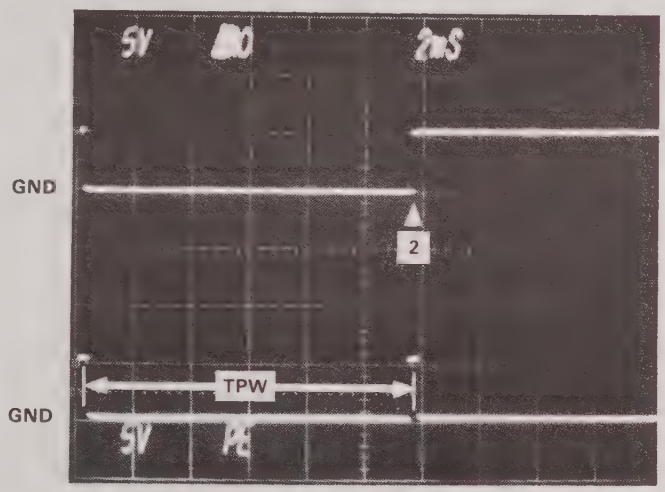


5

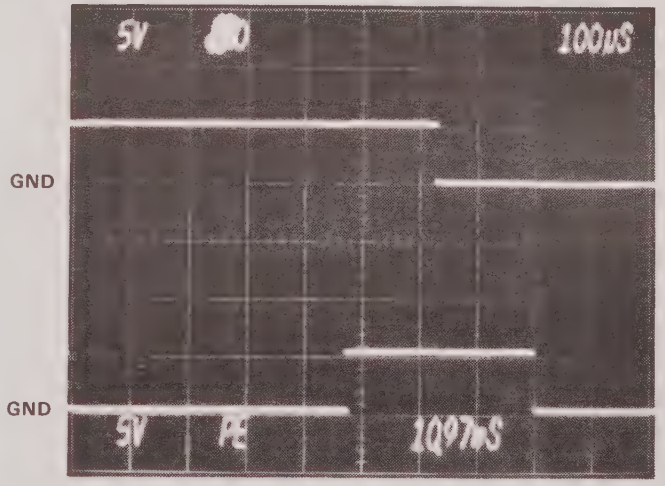
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MAS	10-20-83

DATA I/O

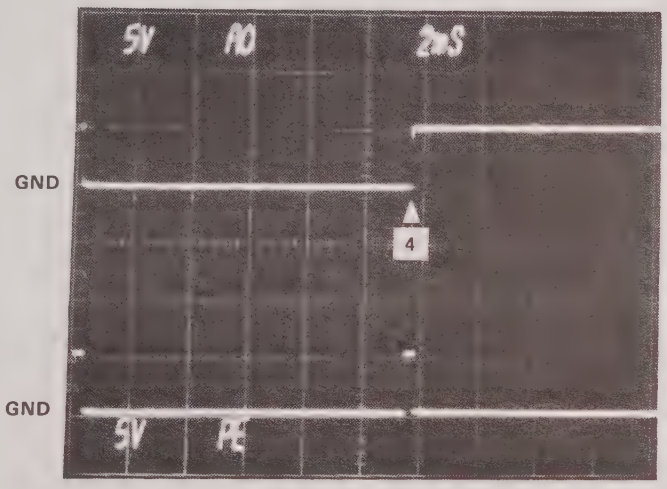
TITLE: TIMING DIAGRAM FAMILY CODE AF		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.
SCALE		SHEET 2/2


5V
2mS
GND
2
TPW
GND
5V
PE

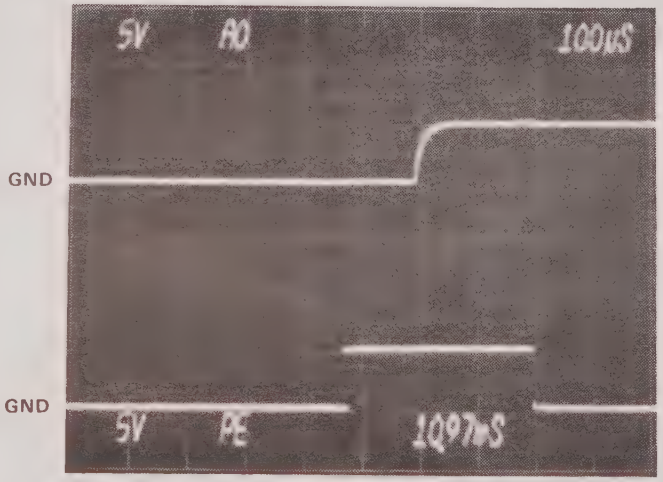
1


5V
100µS
GND
GND
5V
PE
1Q97mS

2


5V
AO
2mS
GND
4
GND
5V
PE

3


5V
AO
100µS
GND
GND
5V
PE
1Q97mS

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*
7. *Photos 5 and 6 are erase waveforms.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.00	5.25	V	
	VEE	9.0	12.0	15.0	V	
	TPW	9.0	-	15.0	ms	
	TD	2	-	-	µs	
	TR	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MJS	10-28-83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE B3

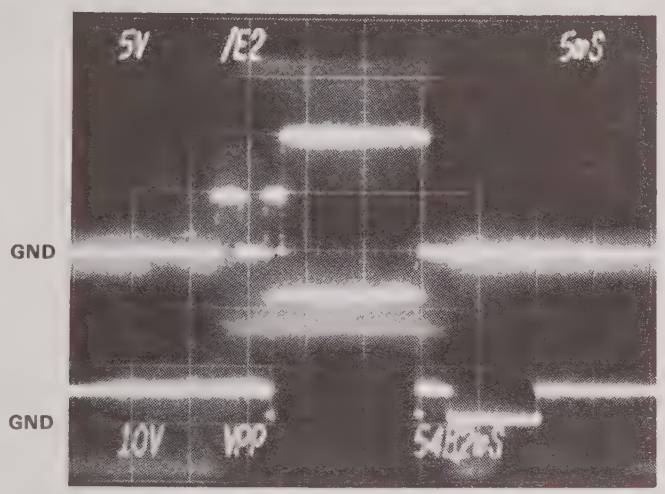
DRAWN BY:

CHECKED BY:

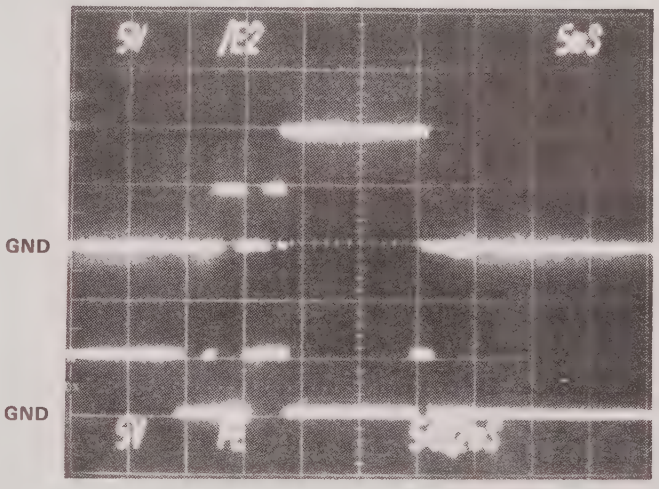
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2



5

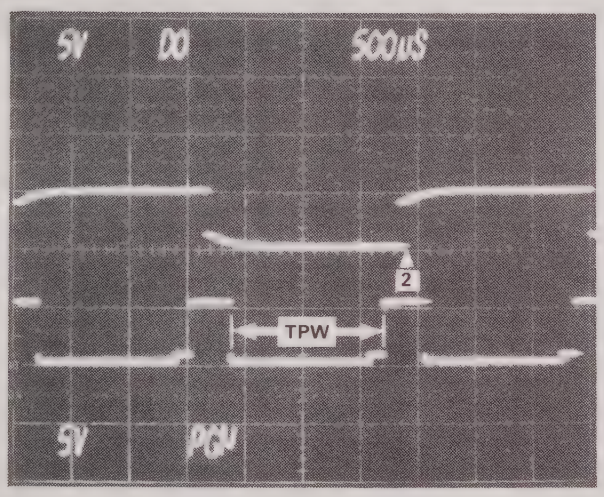


6

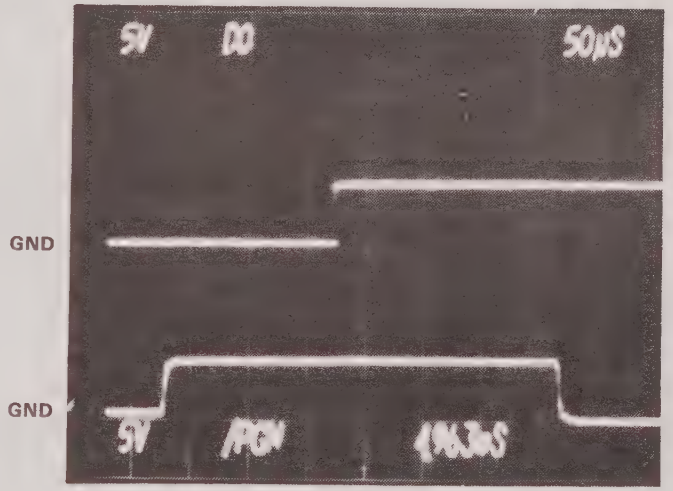
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		[illegible]	10-28-83

DATA I/O

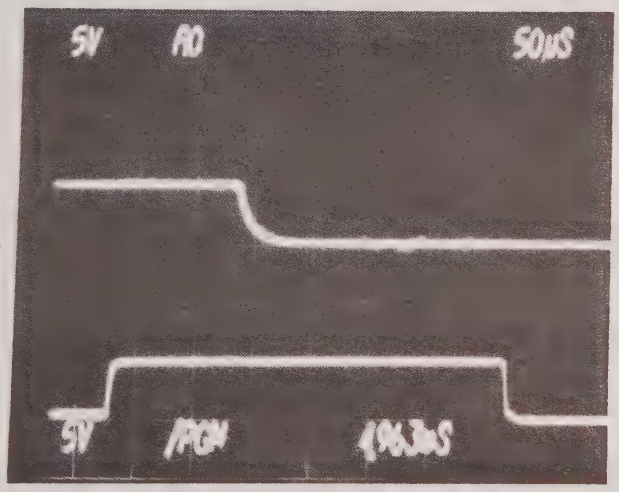
TITLE: TIMING DIAGRAM FAMILY CODE B3		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.
SCALE		SHEET 2/2


5V DO 500µS
GND
2
TPW
GND
5V PGM

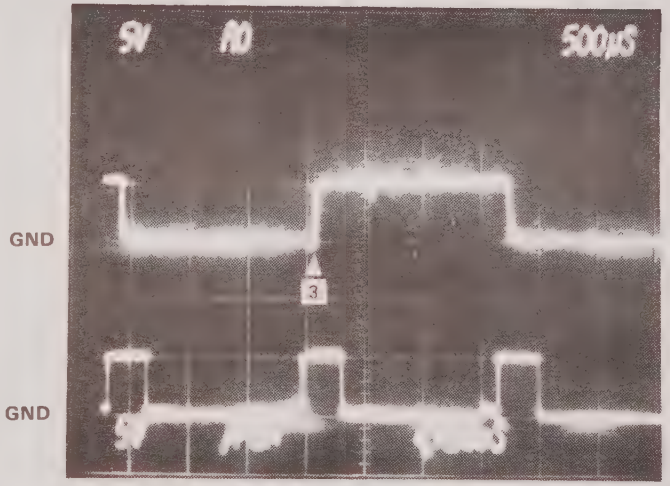
1


5V DO 50µS
GND
GND
5V PGM 1963µS

2


5V AO 50µS
GND
GND
5V PGM 1963µS

3


5V AO 500µS
GND
3
GND

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*
7. *Photo 5 is erase waveform.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
	VCCP	4.75	5.0	5.25	V	
	VPP	4.75	5.0	5.25	V	
	TPW	0.9	1.0	1.1	ms	
	TD	2	-	-	ms	
	TR	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MTS	10-28-83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE B9

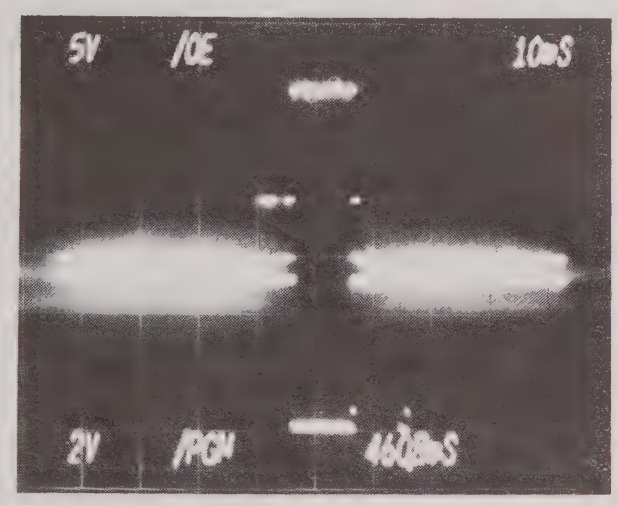
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2



GND

GND

5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MDS	10-28-83

DATA I/O

TITLE

TIMING DIAGRAM
FAMILY CODE B9

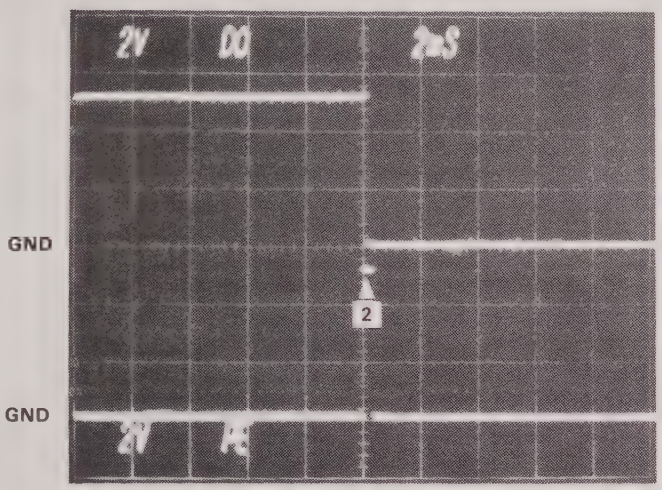
DRAWN BY:

CHECKED BY:

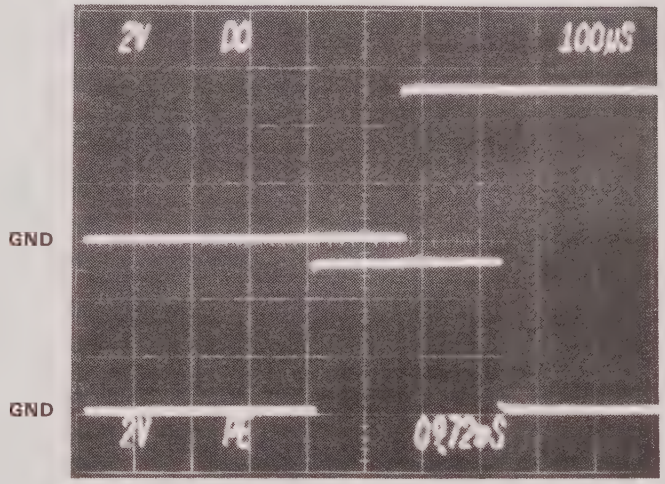
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

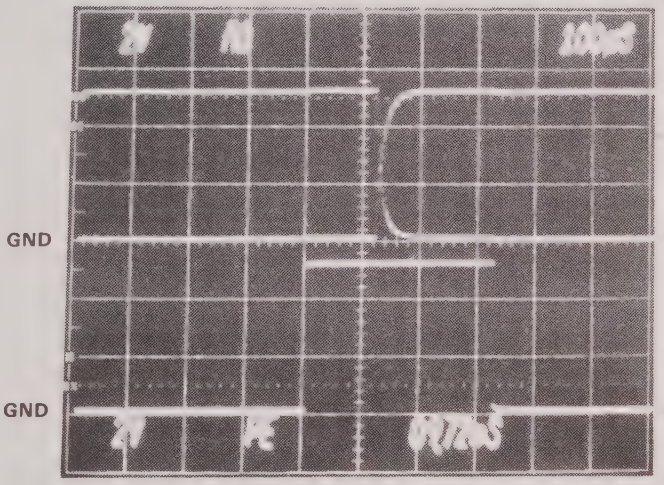
SHEET 2/2


2V
DC
2mS
GND
2
GND
2V
AC

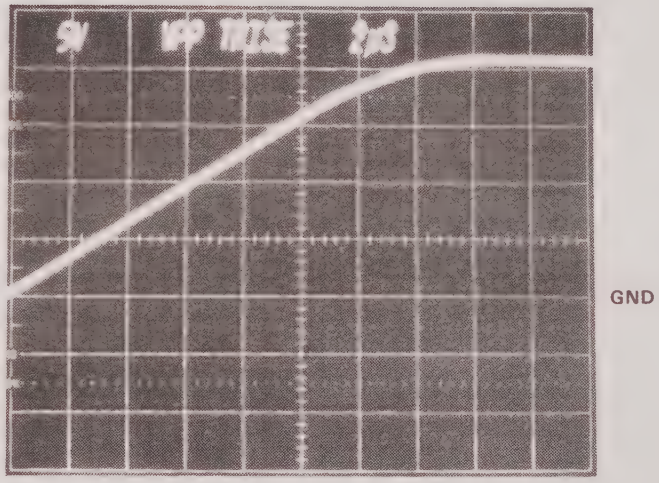
1


2V
DC
100µS
GND
GND
2V
AC

2


GND
GND
2V
AC

3


GND

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
	VCCP	4.75	5.00	5.25	V	Not Shown
	VPP	24	25	26	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	9.8	10	10.2	ms	
	TD	2	-	-	µs	
	TR	50	-	-	ns	
	TF	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MLS	10-28-80

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE BD

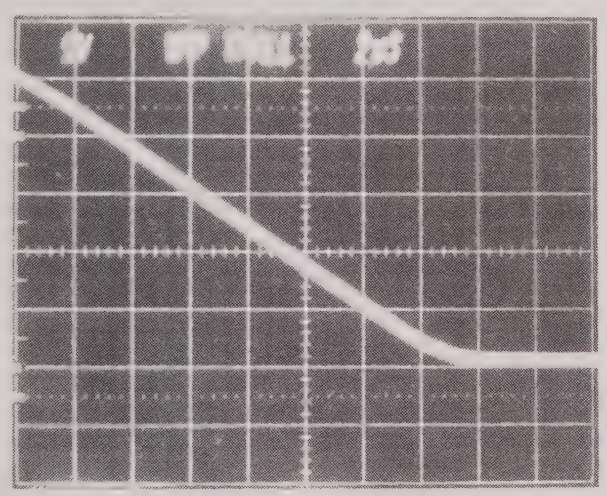
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2



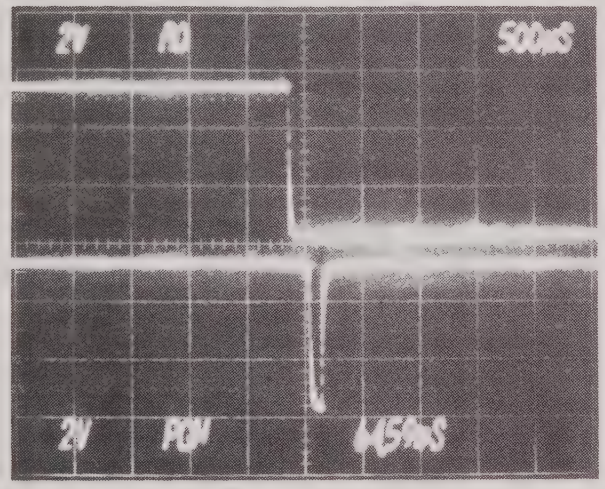
GND

5

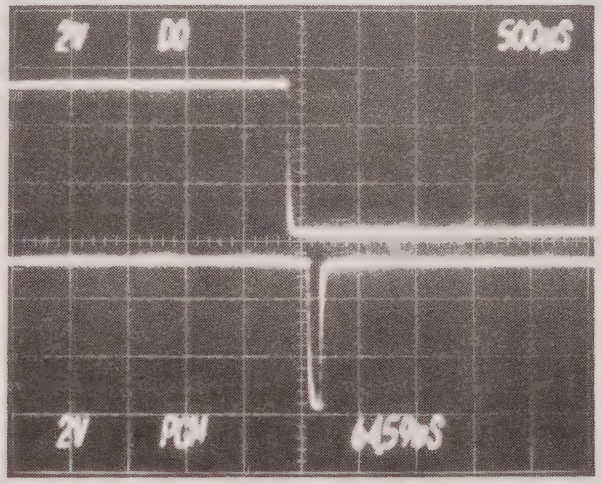
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		JDS	10-24-83

DATA I/O

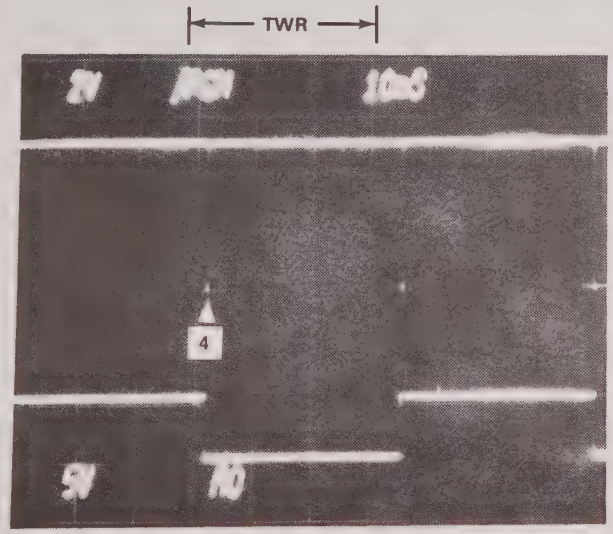
TITLE: TIMING DIAGRAM FAMILY CODE BD	DRAWN BY:	
	CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.:
SCALE		SHEET 2/2


2V
A0
500µS
2V
PON
4.45mS

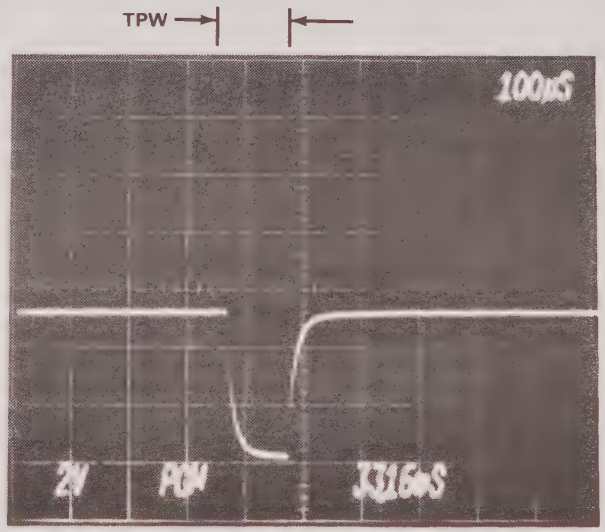
1


2V
D0
500µS
2V
PON
4.45mS

2


TWR
2V
PON
10mS
4
5V
A0

3


TPW
100µS
2V
PON
3.16mS

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with hex AA, 55 pattern.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
	VCCP	4.75	5.0	5.25	V	Not Shown
	TPW	200	-	-	ns	
	TWR	30	-	-	ms	
	TD	2	-	-	ms	
	TR	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MP S	10/28/83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE BF

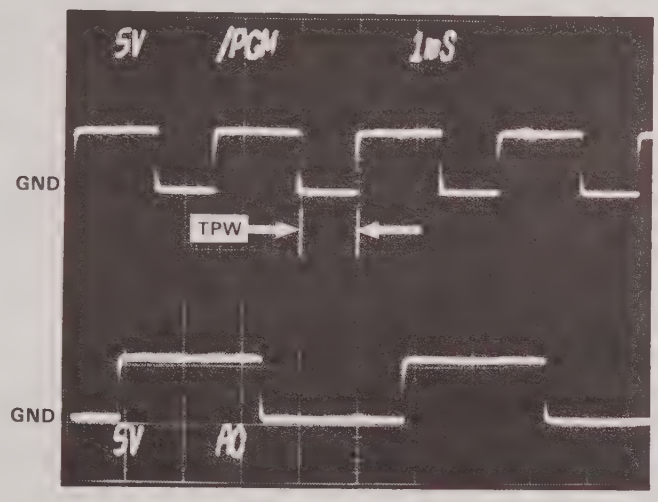
DRAWN BY:

CHECKED BY:

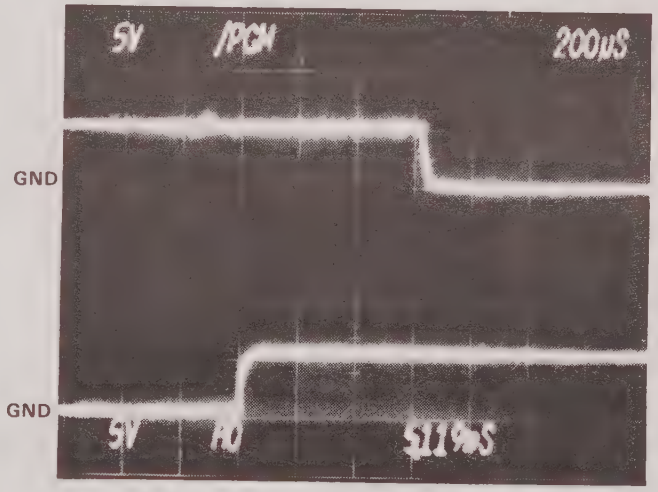
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

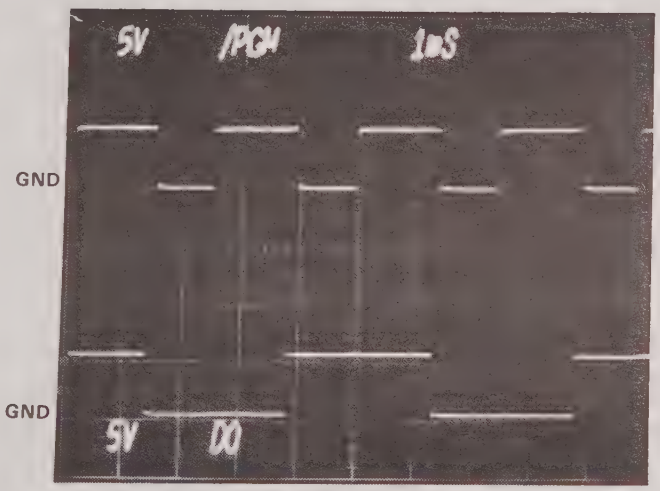
SHEET 1/1


5V
/PCM
1uS
GND
TPW
GND
5V
A0

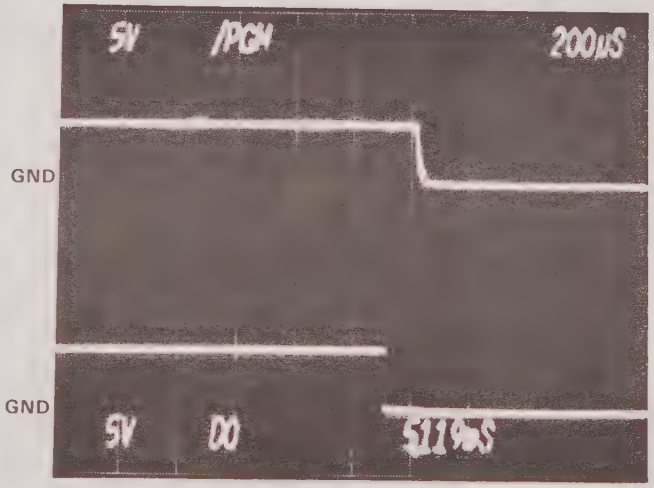
1


5V
/PCM
200uS
GND
GND
5V
A0

2


5V
/PCM
1uS
GND
GND
5V
D0

3


5V
/PCM
200uS
GND
GND
5V
D0

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
	VCCP	5.75	6.0	6.25	V	
	VPP	12.5	13.0	13.5	V	
	TPW	.9	1	1.1	ms	
	TD	2	-	-	us	
	TR	50	-	-	ns	
	REJECT		25		PULSES	
	OVERPROGRAM		2		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MS	10-26-83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE C1

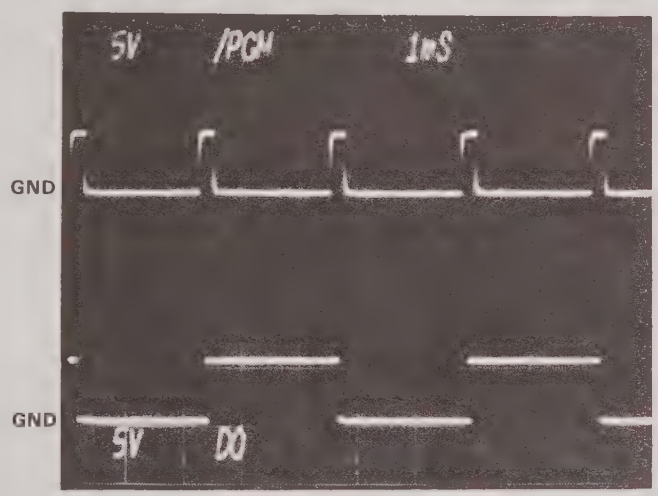
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

SHEET 1/2



5

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MDS.	10-24-83

DATA I/O

TITLE

TIMING DIAGRAM
FAMILY CODE C1

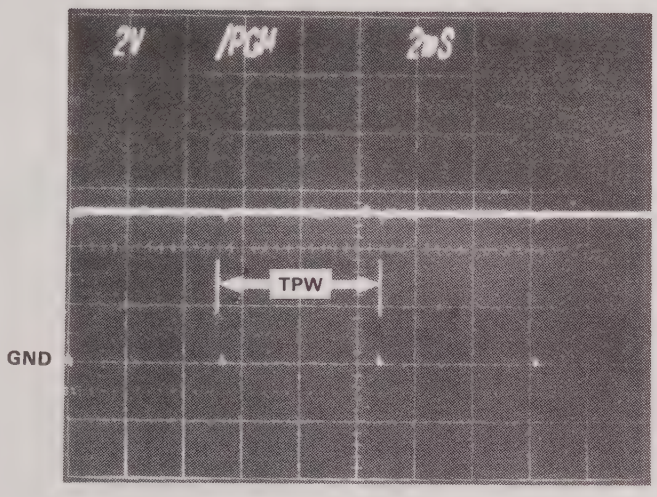
DRAWN BY:

CHECKED BY:

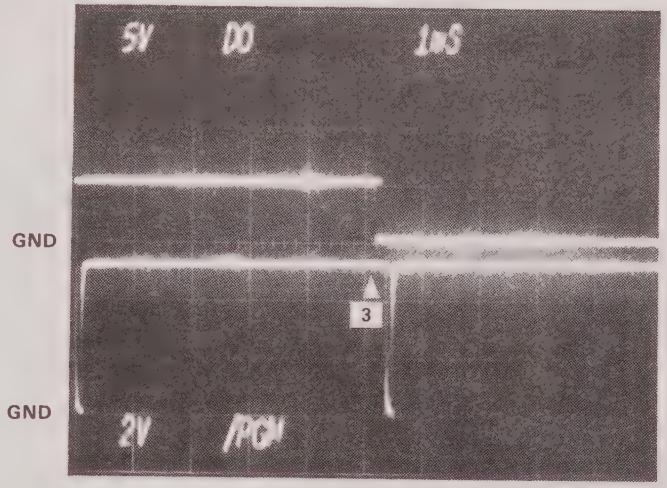
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

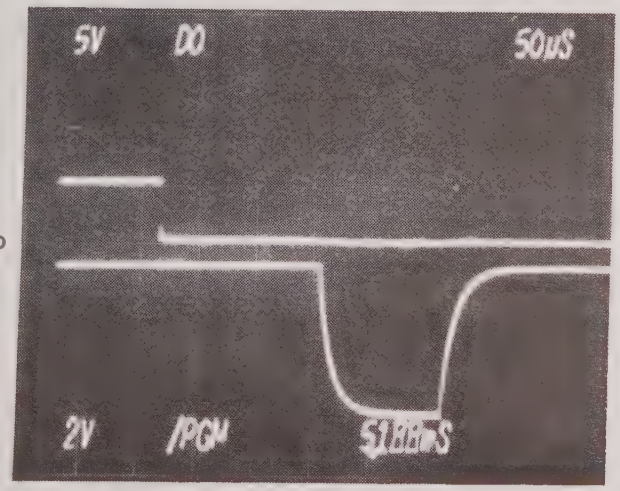
SHEET 2/2


2V
/PCM
2mS
TPW
GND

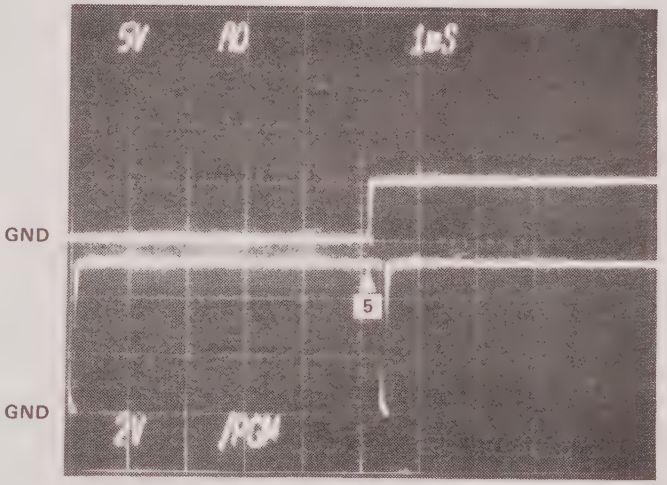
1


5V
DO
1mS
GND
3
GND
2V
/PCM

2


5V
DO
50uS
GND
GND
2V
/PCM

3


5V
AO
1mS
GND
5
GND
2V
/PCM

4

NOTES

1. *Oscilloscope trigger point: As noted on photograph.*
2. *Oscilloscope ground reference: GND contact on socket 11.*
3. *The Pinout Chart, Figure 5-5, indicates which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Load RAM with alternating $AA, $55 pattern.*
7. *Photos 6 and 7 show chip erase.*

WAVEFORM VARIABLES

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	TPW	-	5	-	ms	
	TD	2	-	-	ms	
	TR	50	-	-	ns	
	REJECT		1		PULSES	
	OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		MPS	11-14-83

DATA I/O

TITLE
TIMING DIAGRAM
FAMILY CODE C3

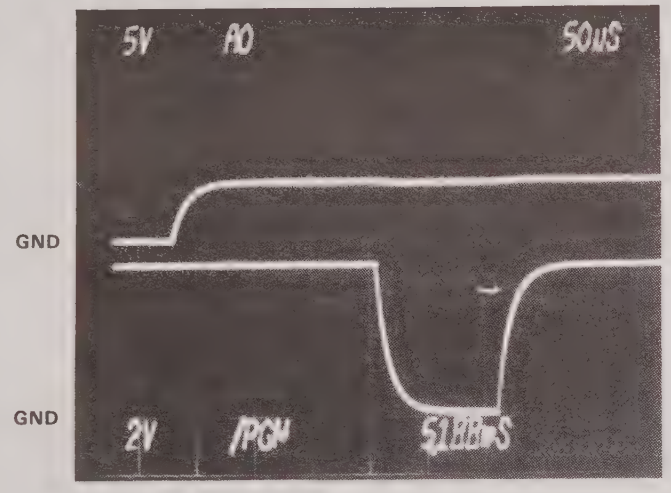
DRAWN BY:

CHECKED BY:

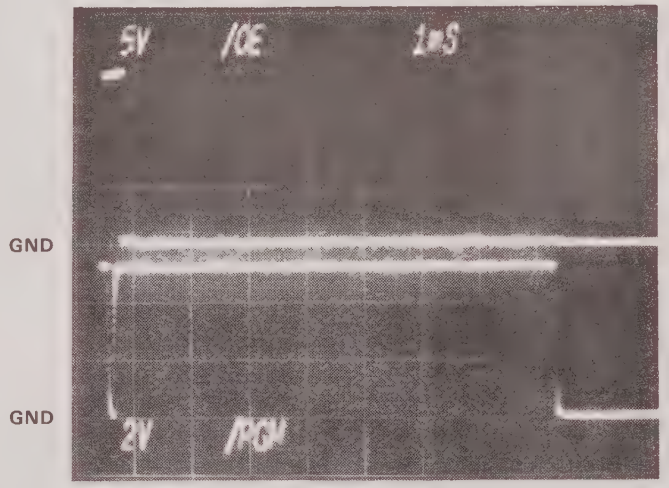
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	

SCALE

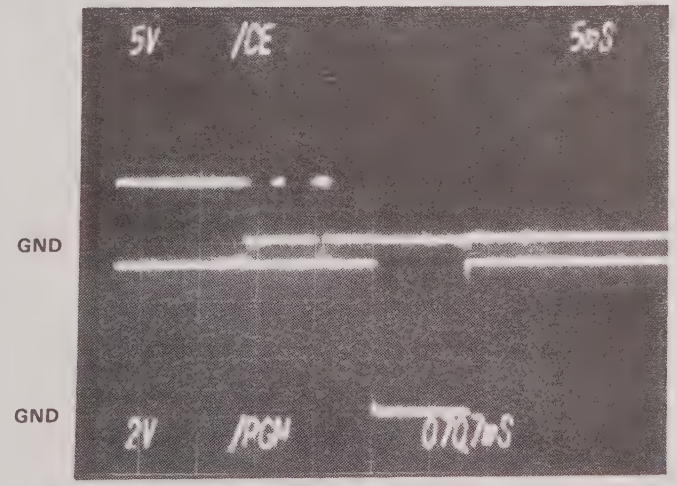
SHEET 1/2


5V
A0
50uS
GND
GND
2V
/PGM

5


5V
/CE
1mS
GND
GND
2V
/PGM

6


5V
/CE
5nS
GND
GND
2V
/PGM

7

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN# 4978		JMS	11-14-83

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODE C3		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.
SCALE		SHEET 2/2

5-91
10-990-0120

SECTION 6
MAINTENANCE

6.1 INTRODUCTION

The primary maintenance requirement is for periodic cleaning of the air filters to make sure that airflow is not impeded. Except for this precaution, check the outside of the unit routinely for dust or dirt, and check the inside for cables or other components that may have become unseated.

6.2 CLEANING

Clean the outside of the unit with a mild detergent on a damp cloth or brush. Never use caustic or abrasive agents; these will damage the programmer.

Periodically inspect each socket and its contacts for accumulated dirt and debris. Also inspect each contact for smooth opening and closing. Dirt and debris can usually be removed with compressed air.

The socket itself is contructed of polyphenylene material and should be cleaned only with methyl alcohol, Freon TE™, or detergent and water. Do not lubricate.

6.3 INSPECTION

Check cable connections, card seating, mounting of socketed components, etc., for shorts, opens or unstable continuity. Use particular care if you find heat-damaged components. It is important to find and correct the cause of overheating in order to prevent recurrence of the damage. If you find parts damaged through overheating, consult Section 4, Troubleshooting.

SECTION 7
CIRCUIT DESCRIPTION

7.1 INTRODUCTION

This section describes the programmer's circuitry. It discusses the following topics:

- General Architecture
- Address Map
- Components
- Assembly Cabling
- Circuitry Functions

7.2 ARCHITECTURE

The programmer is a microprocessor-based system using bus architecture. It is designed around a 6809E microprocessor chip. The processor is located on the 6809E CPU board (701-1647-001). Figure 7-1 is the system block diagram.

The circuitry of the programmer's main components is described in sections 7.4 through 7.14. Block diagrams are provided for each of these components. Schematics are provided in Section 8.

7.2.1 THE BUS

The modular bus consists of a 16-bit address bus, 8-bit data bus, power supply lines and control lines. These are detailed in Table 7-1. All communications between portions of the circuitry are handled in the same manner over this bus. Timing of read and write operations is shown in Figure 7-2.

7.2.2 ADDRESS MAP

The address map of Table 7-1 shows the location, in hexadecimal, of each decoded function of the programmer.

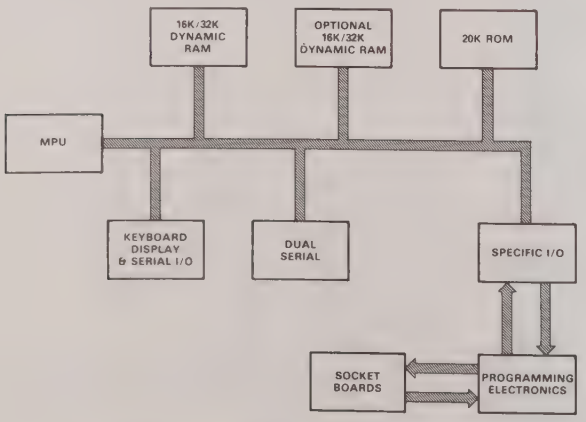


Figure 7-1. System Block Diagram

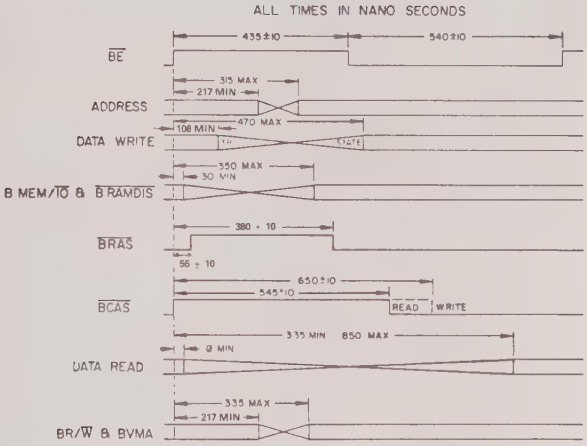


Figure 7-2. Modular Bus

7.3 COMPONENT LAYOUT

Figure 7-3 shows the cabling interconnection between major assemblies on the programmer.

Table 7-1. Address Map

ADDRESS	FUNCTION	ADDRESS	FUNCTION
8400	ACIA 2	8408	TIMER START
8402	ACIA 3 (unused)		OF 8253 REG
8408	ACIA 1	84D0	PRMWR
840A	Keyboard/Display	84D1	LOADLD
8410	SWA 0A2	84D2	HOADLD
8411	SWA 0A3	84D3	OEREG
	(unused)	84D4	PRMRD
8414	SWA 0A1	84D5	LEDWR1
8400	PAGE 1	84D6	LEDWR2
8401	PAGE 2	84D7	LEDWR3
8402	SWCH 1	84D8	DAC1
	PROM Type	84D9	DAC20
8403	SWCH 2 SPEC.	84DA	DAC21
	FUNC TSTIM -	84DB	DAC22
	Bit 7 LOW FOR	84DC	DAC23
	TIMER INT.	84DD	DAC28
8406	CLRTIM -	84DE	PRRDEN
	CLEARS TIMER	84DF	ADACLD
	INT.		
8407	STRTIM -		
	STARTS TIMER		

7.4 MAIN COMPONENTS

The following paragraphs describe the circuitry of the programmer. References are made to individual block diagrams of certain circuit boards. The schematic for each board can be located in Section 8, Schematics.

7.5 POWER SUPPLIES

Figure 7-4 is a block diagram of the programmer's power supply components.

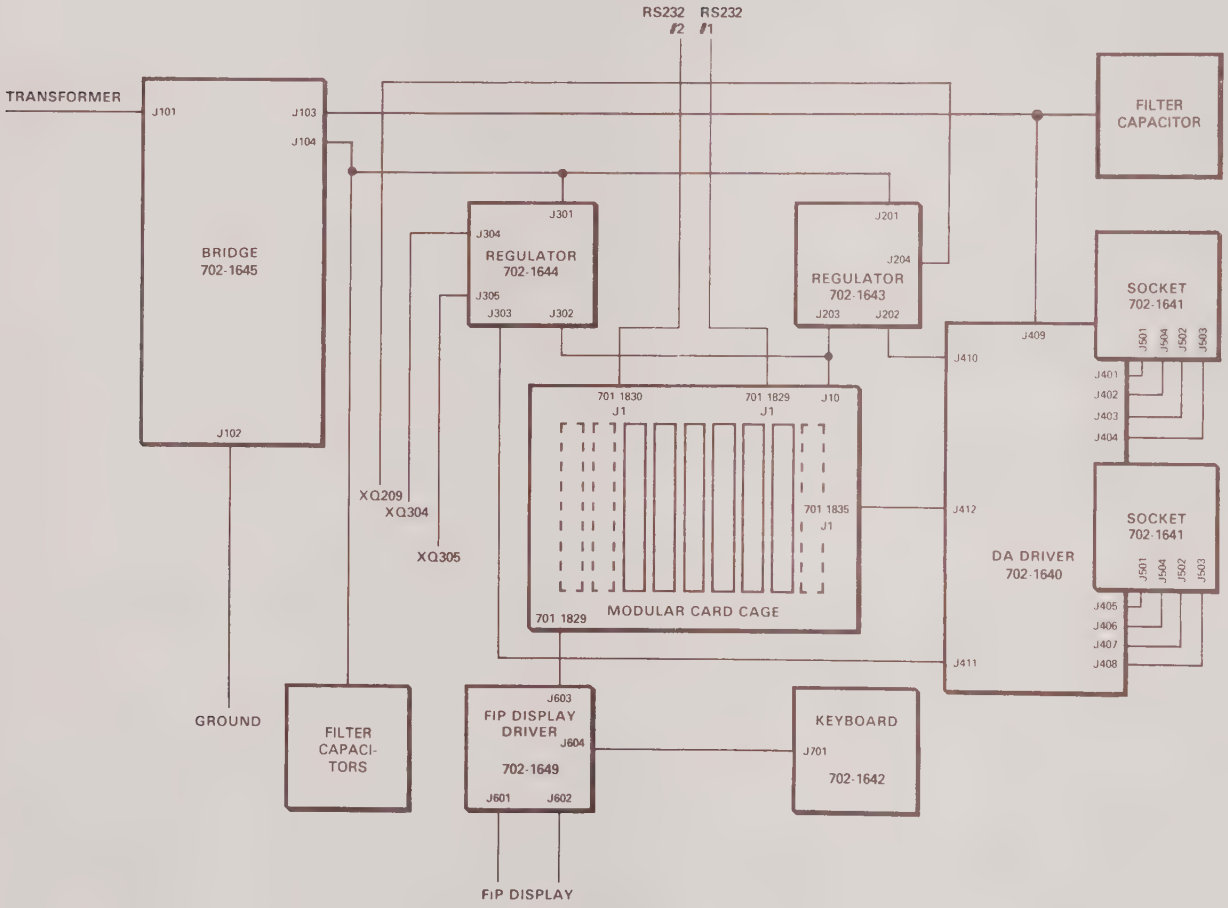


Figure 7-3. Interconnection Diagram

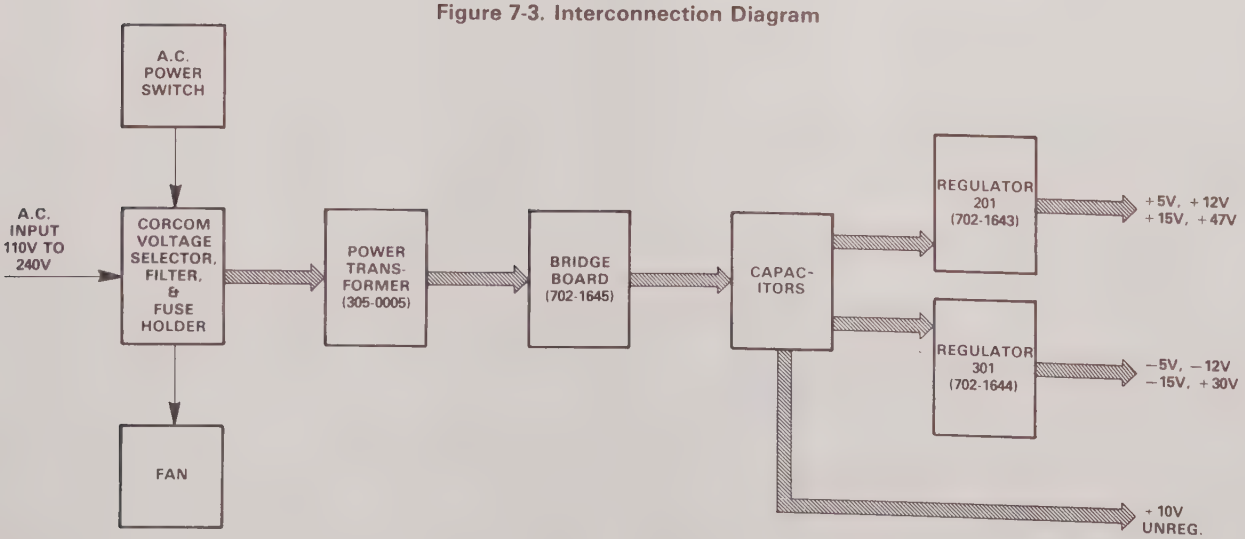


Figure 7-4. Block Diagram, Power Supply Components.

Voltage Selector

The voltage selector adapts the unit to the line voltage by means of a printed circuit board inserted in any of four ways to connect a particular combination of the transformer primary windings to the input line. A slow-blow fuse is also inserted in the CORCOM to provide short-circuit protection against failure of the power supply.

Transformer Secondary

The secondary is presented via connector J101 to the power input of the Power Supply Bridge board.

Power supply rectification and fusing are accomplished on this board. Table 7-3 lists the correct fuses for normal operation and Figure 7-5 shows where the fuses are located.

Table 7-2. Fuse Requirements on the Power Supply Bridge Board

FUSE LOCATION	FUSING VALUE
F1	2 amp slow-blow
F2	2 amp slow-blow
F3	1 amp slow-blow
F4	1 amp slow-blow
F5	10 amp
F6	10 amp
F7	8 amp
F8	8 amp

Regulator 201 Board

The Regulator 201 board (P/N 702-1643) supplies regulated +5 V, +12 V, +15 V and +47 V. These voltages are derived from the unregulated +10 V, +22 V and the +67 V supplies.

The overcurrent circuitry senses for the +5 V, +15 V and +47 V. These supplies are used to form an OR gate which provides foldback current limiting. This is accomplished by turning on Q1, which in turn sustains base drive to Q6, keeping Q1 on. With Q1 on, the references for the +47 V, +15 V and +5 V regulators are clamped to ground. In addition, the adjustment terminal for Q209, the +12 V regulator, is clamped to ground. This insures zero (or near zero) output under overcurrent conditions. The base of Q1 is also driven from a −5 V sense line from the Digital/Analog Driver Board (702-1640). This insures that the +5 V, +12 V, +15 V and +47 V supplies are shut down if −5 V is lost for any reason.

The +47 V regulator consists of zener diode (CR14) acting as a reference for the pass transistor (Q9). If an overcurrent exists, Q6 senses the increased voltage across R27 and starts to conduct. This is the +5 V regulator's overcurrent sense output.

The +5 V regulator consists of a shunt regulator (VR1) driving transistor Q5. This transistor in turn drives a pair of pass transistors (Q3 and Q4). Feedback is provided to the shunt from the Remote Sense line through precision resistor R10. If an overcurrent exists, Q2 senses the increased voltage across R3 and starts to conduct. This is the +5 V regulator's overcurrent sense output.

The +15 V regulator consists of a shunt regulator

F1 = 2 amp slow blow
F2 = 2 amp slow blow
F3 = 1 amp slow blow
F4 = 1 amp slow blow
F5 = 10 amp
F6 = 10 amp
F7 = 8 amp
F8 = 8 amp

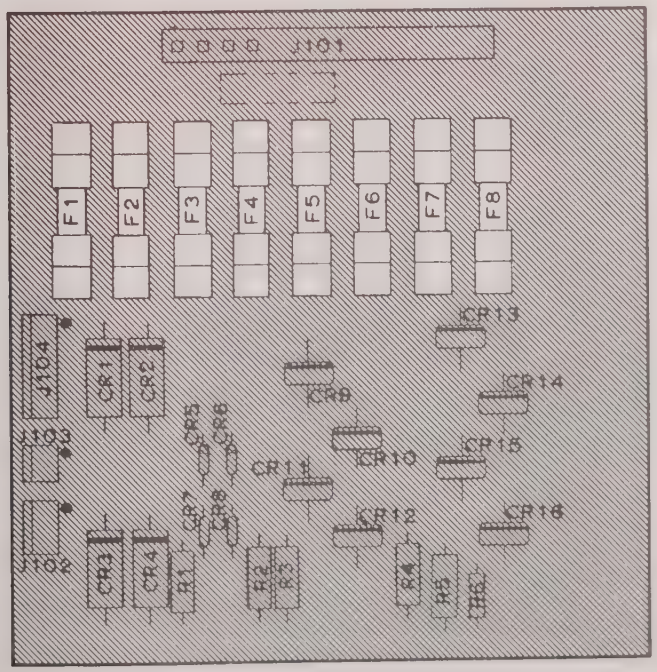


Figure 7-5. Fuse locations on the Power Supply Bridge Board.

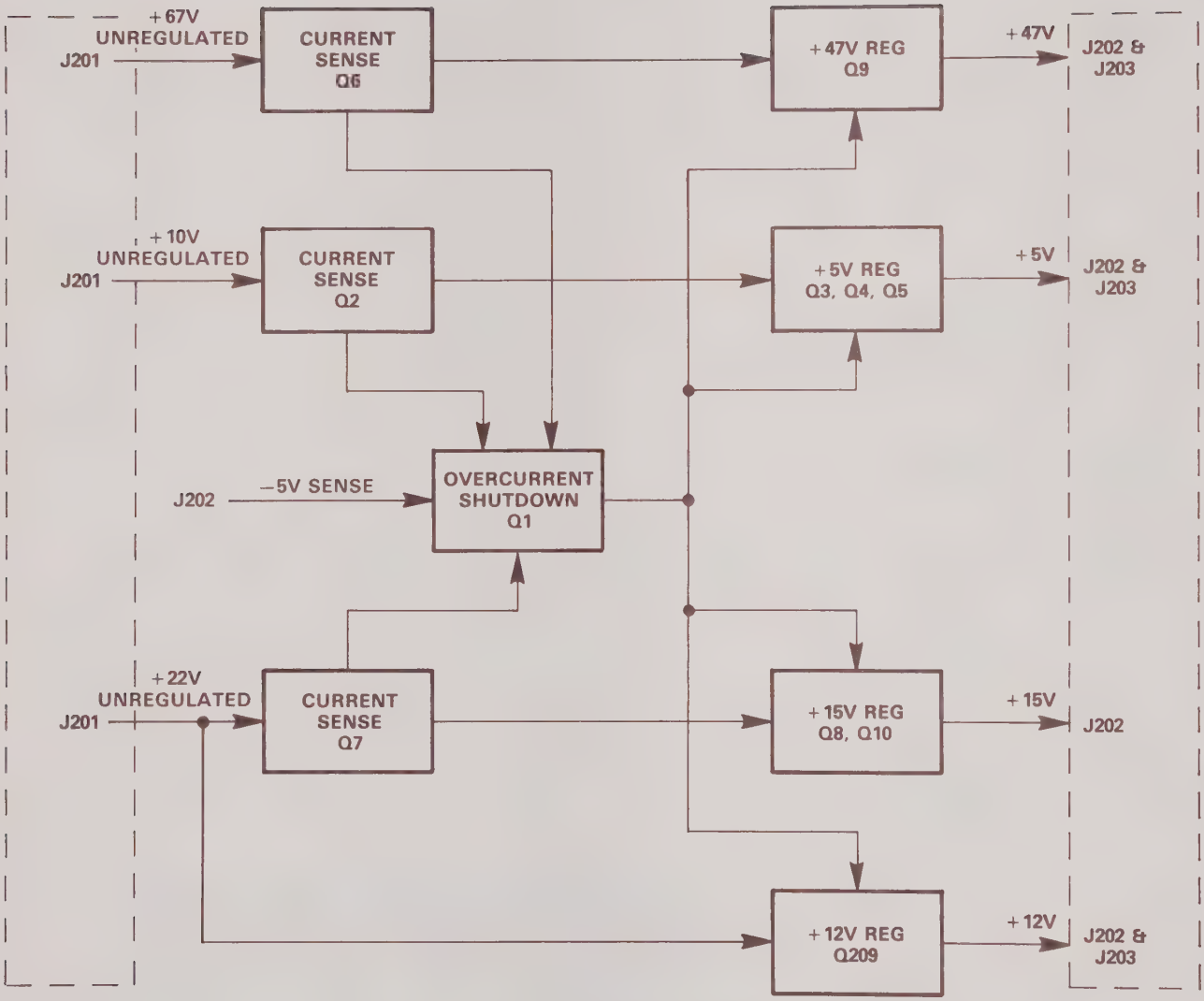


Figure 7-6. Block Diagram, Regulator 201 Board

(VR2) driving transistor Q8. This transistor in turn drives pass transistor Q10. Feedback is provided to the shunt regulator through precision resistor R29. If an overcurrent exists, Q7 senses the increased voltage across R32 and starts to conduct. This is the +15 V regulator's overcurrent sense output.

The +12 V regulator consists of a three-terminal adjustable regulator (Q209) which is programmed by the precision resistors (R33, R34 and R35) providing +12 V output. This regulator has internal current limiting.

Regulator 301 Board

The Regulator 301 board (P/N 702-1644) supplies regulated +30 V, −5 V, −12 V and −15 V. These voltages are derived from the unregulated +42 V −22 V supplies. These regulators are standard three-terminal regulators employing internal current limiting. Figure 7-7 provides a block diagram of the Regulator 301 board.

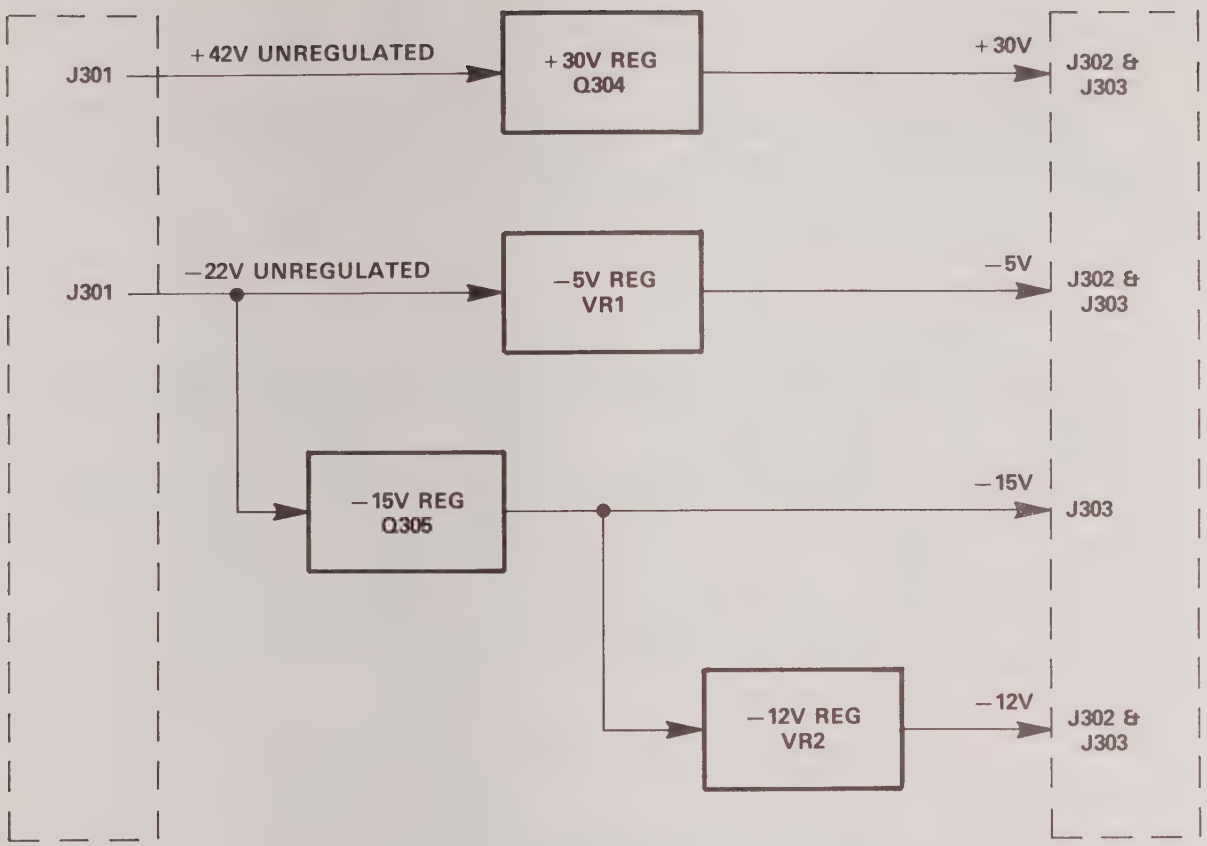


Figure 7-7. Block Diagram, Regulator 301

7.6 MOTHERBOARD

Refer to the schematics in Section 8.

The Mother Board (P/N 702-0192) contains nine female card connectors (J1 - J9.)

Each socket connects dual rows of 28 pins. The power input connector for the Mother Board uses the 12-pin connector, J10.

The Mother Board is common-bused on all line with large traces used for the +5 V supply and ground. Filters are used for normal logic levels +5 V, −5 V, and +12 V. All bus lines are unterminated, relying on tri-stated drivers on each module to accomodate level controls.

7.7 6809E CPU BOARD

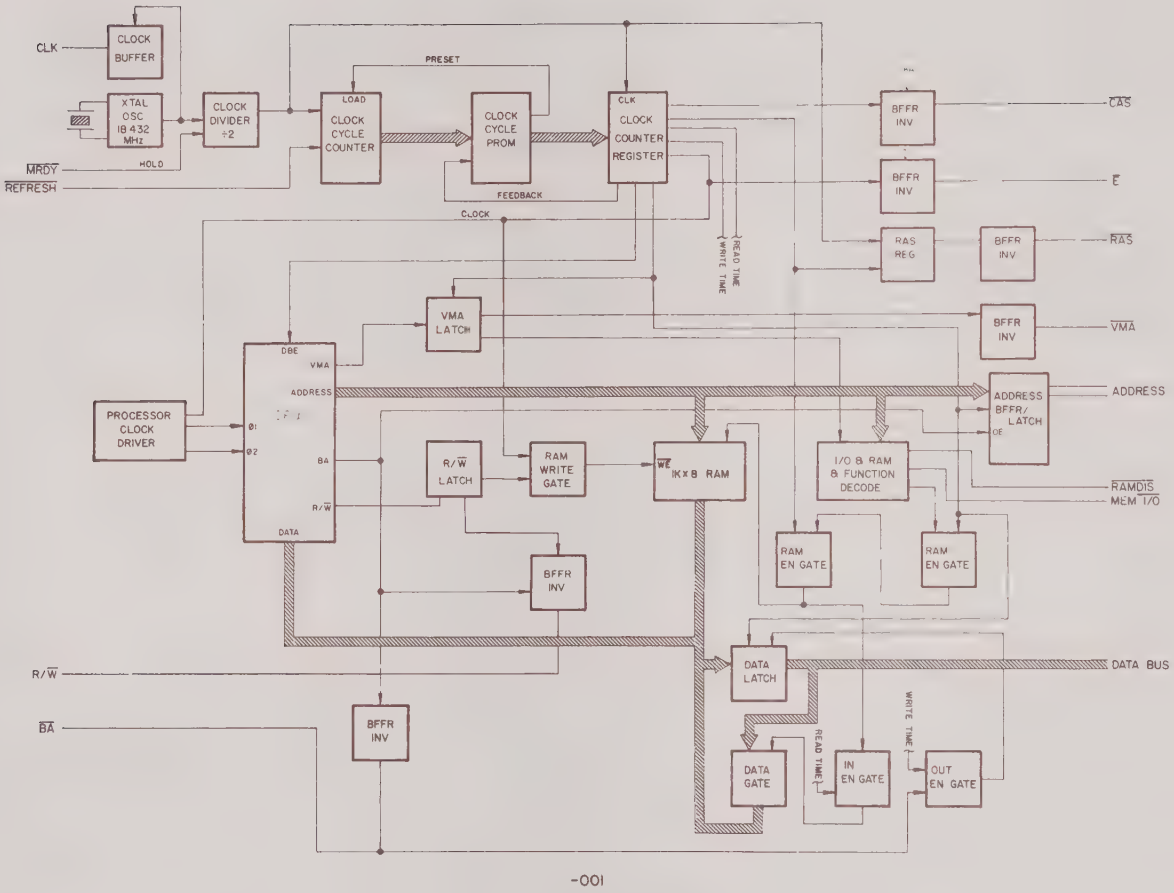
The 6809E CPU Board (P/N 701-1647-001) is the master controller of the system. It contains a 6809E microprocessor (U4), 1Kx8 scratch RAM (U8 and U12), system timing circuitry and a power-on-reset circuit. The board sends addresses, data and control signals to the rest of the system.

System Timing. Refer to Figure 7-2. System timing is derived from an 18.432 MHz signal provided by crystal Y1 and Y2 inverters of U1. This signal is divided by JK flip-flop U3 to provide the clock for the 4-bit counter, U5. The outputs from this counter address and 32Kx8 PROM (U9). This PROM is programmed to produce the required timing signals. The outputs of the PROM are sampled by latch U13, and the outputs of this latch constitute the timing signals used throughout the circuit. One output of the PROM is fed back to the counter. This is used to reset the count sequence.

The clocks to the 6809E are provided by an open collector driver (U2). The microprocessor is clocked at 1.024 MHz.

Address Bus. The microprocessor address bus is buffered by transparent latches U11 and U16. The enable for these latches is derived from the timing logic. Address decoding is provided by the 256x4 PROM, U7. In addition to decoding the static RAM it also provides a decode (MEM/$\overline{IO}$) which is used to simplify I/O decoding in the rest of the system.

The reset to the processor is provided by the dual one-shot (U15). One half of this produces a long reset pulse during power-on. The other half produces a short reset pulse when the bus line Reset goes low and back to high again. This bus line has a passive pull-up to facilitate wired-OR. Figure 7-2 illustrates the timing relationships of the bus as they appear at the backplane connector (JXX).



-001

Figure 7-8. Block Diagram, 6809E CPU Board

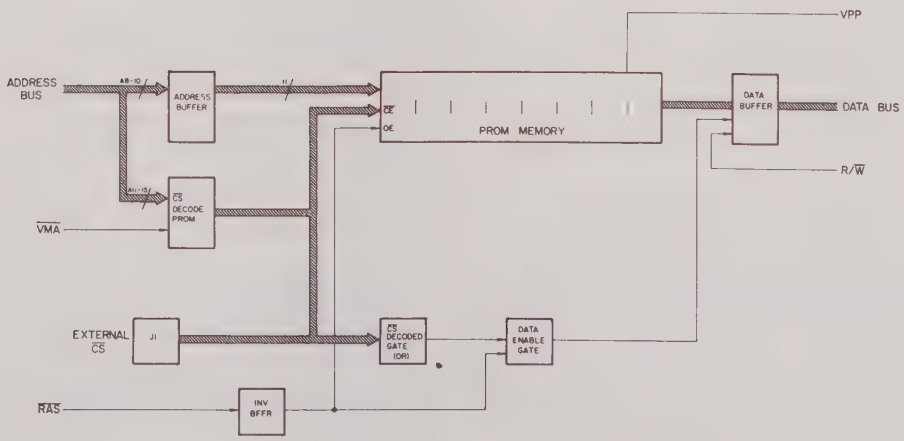


Figure 7-9. Block Diagram, PROM Card

7.8 PROM CARD

Refer to Figure 7-9.

This board contains the necessary decoding and buffering to provide up to 32K of EPROM memory. The devices used are 2732s (4Kx8). Decoding is provided by the 32x8 PROM U12. The row address strobe (RAS) timing signal from the bus enables the bidirectional data bus buffer (U6) if one of the PROMs, U1 through U9, is selected. Selection of one of the PROMs is detected by the 8-input gate, U14.

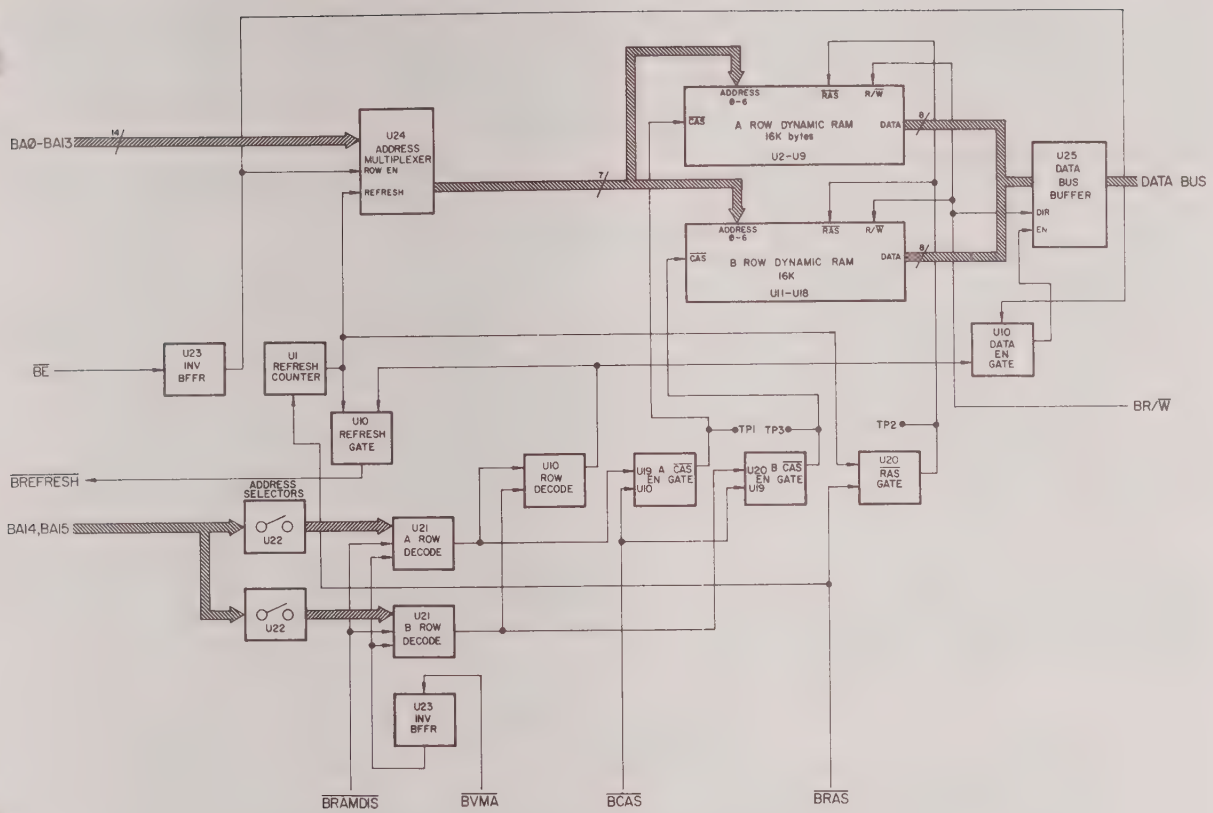


Figure 7-10. Block Diagram, 16/32K Dynamic RAM Board.

7.9 16/32K DYNAMIC RAM BOARD

Refer to Figure 7-10.

The 16/32K Dynamic RAM Board (P/N 701-1827) consists of eight 16Kx1 memory chips (U2 through U9.) Locations U10 through U18 provide space for an additional 16K of RAM. An address multiplexer (MUX), U24, generates column and row addresses and maintains Count and Refresh signals. Data bus buffer U25 is a bidirectional buffer which passes data in whichever direction is commanded by the input on pin 1. An eight-position address selection switch (U22) decodes the starting address for each 16K bytes of RAM.

The RAM memory is always isolated from the system bus except when addressed to read or write data. At all other times it sustains itself with refresh cycles sent by the timing control lines of $\overline{RAS}$ and $\overline{CAS}$.

Seven address lines connect to MUX U24. The MUX is series-connected to resistors RP1 and RP2 to prevent any current surge. This eliminates the danger of damaging the RAMs from negative spikes.

The MUX operates as an address buffer bus isolater which sends high-and-low order addresses to the RAMs in two cycles. The MUX has an input for Row Enable (E), seven address lines, and $\overline{Count}$ and Refresh lines. Each $\overline{RAS}$ input clock advances the internal refresh counter of the MUX and inhibits the refresh gate. This allows the MUX refresh address to advance.

The refresh gate output is used to stretch the E pulse (all bus functions during E of the clock cycle.)

7.10 KEYBOARD DISPLAY AND SERIAL I/O CARD

Refer to Figure 7-11.

The Keyboard Display and Serial I/O Card (P/N 701-1829), also known as the Keyboard/Display Interface and Asyncronous Serial Port Card, controls the keyboard/display interface and serial port 1. Its major components are described in the paragraphs below.

Keyboard/Display Controller. The separate Read and Write signals are generated by using U6 to gate R/$\overline{W}$ (from P1 pin 13) and E (from P1 pin 7.) Because the IRQ active level of U3 is opposite that of the 6809E processor, and IRQ driver (U7 pin 4) is used to generate an interrupt whenever a key is pressed. This chip also interfaces with a 34-pin ribbon cable connector which drives the front panel logic.

ACIA. The Keyboard Display and Serial I/O Card contains one 6850 ACIA (U8) which interfaces with the data bus via a data buffer (U14.) Decoder U13 uses address lines A0 through A7 for mapping, gated with MEM/$\overline{IO}$ and $\overline{RAS}$. Output Ø2 of the decoder is active for all decoded functions on the board and enables the data buffer. The direction of the buffer is controlled by R/$\overline{W}$. Each ship is enabled by a separate decode line as well as the status gate.

Baud Rate Generator. The bus clock (at P1, pin F) is

applied to the counter network (U5 and U11), which provides baud rates from 110 to 9600. The eight-segment DIP switch, U1, is used for baud rate selection. A divide-by-eleven counter (U10) reduces the 1200 baud output of U5 to 110 baud. U1 provides the selected rate to pins 3 and 4 of the ACIA.

RS232C and 20mA Interface. The ACIA provides Send Data, Request to Send, Receive Data, Clear to Send and Data Carrier Detect lines in TTL levels. The Send and Request to Send outputs are applied to connector J1 through RS232C drivers (U9). These drivers convert the TTL output of the ACIA to RS232C levels. The Receive, Clear to Send and Data Carrier Detect signals are converted to TTL levels from RS232C levels by the U4 receivers.

The interface also includes 20mA send and receive controls which use transistor-level shifter networks. The 20mA Receive line (pin 12) provides an RS232C level on the 20mA Detect line (pin 13). In order to use this function, the 20mA Detect line must be jumpered to RX (pin 3) within the external connector.

7.11 DUAL SERIAL BOARD

Refer to Figure 7-12.

ACIA. The Dual Serial Board (P/N 701-1830) contains two ACIAs (U9 and U12). Each is independent in function and baud rate. These devices interface to the data bus via data buffer U16. Decoder U15 uses address lines A0 through A7 for mapping, gated with MEM/IO and RAS. One output of the decoder D3 is active for all decoded functions on the board, and enables the data buffer. The direction of the buffer is controlled by R/W. Both ACIA U9 and U12 are enabled by one decode line and one address line (A1). The status gates (U10) are enabled by a separate decode line.

Baud Rate Clock. The bus clock (at P1, pin F) is applied to a counter network (U13 and U11) which provides baud rates from 110 to 9600. Two baud rate selectors (U3 and U6) are used to individually select rates for each ACIA. A divide-by-eleven counter (U8) reduces the 1200 baud output of U11 to 110 baud.

RS232C and 20mA Interface. The two ACIAs provide Send Data, Request to Send, Receive Data, Clear to Send and Data Carrier Detect lines in TTL levels. The Send and Request to Send outputs are applied to connectors J1 and J2 through RS232C drivers (U1). These drivers convert the TTL output of the ACIAs to RS232C levels. The Receive, Clear to Send and Data Carrier Detect signals are converted to TTL levels from RS232C levels by the U2 and U7 receivers.

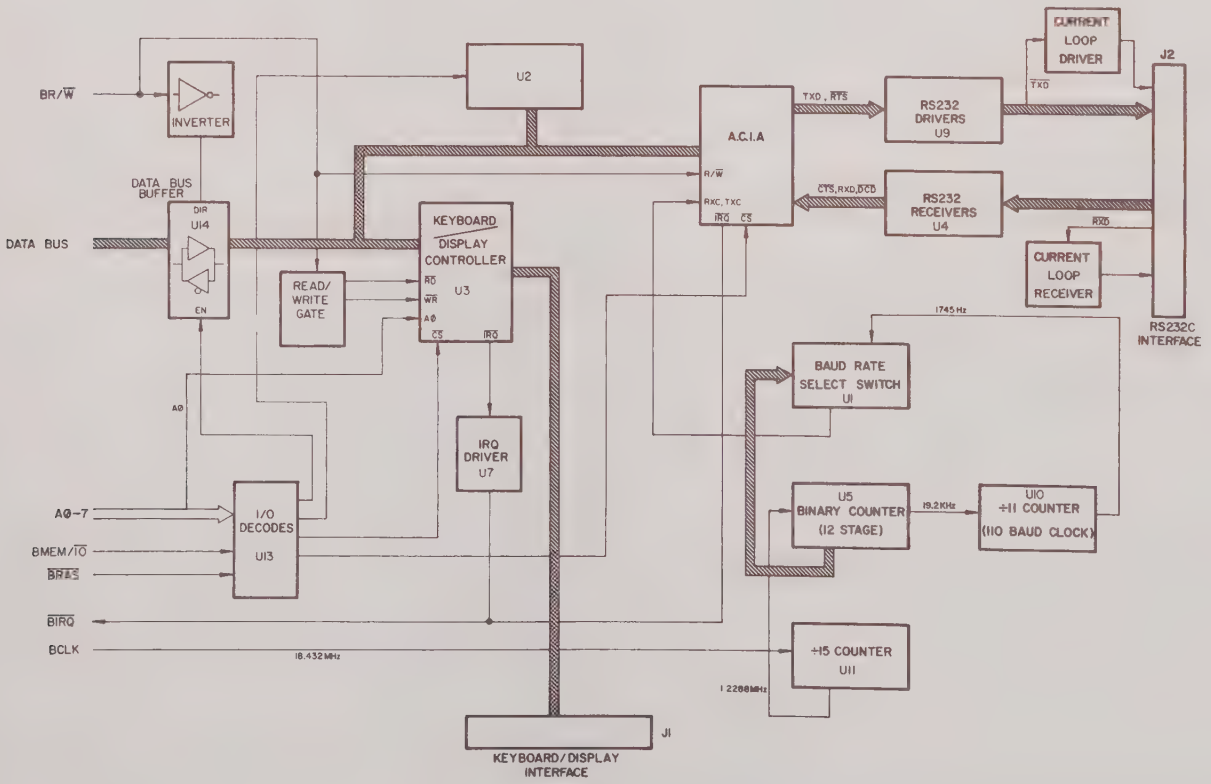


Figure 7-11. Block Diagram, Keyboard Display and Serial I/O Card

The interface also includes 20mA send and receive controls, which use transistor-level shifter networks. The 20mA Receive line (pin 12) provides an RS232C level on the 20mA Detect line (pin 13). In order to use this function, the 20mA Detect line must be jumpered to RX (pin 3) within the external connector.

7.12 DIGITAL/ANALOG DRIVER BOARD (PROGRAMMING ELECTRONICS)

Refer to Figure 7-13.

The Digital/Analog Driver Board (P/N 702-1640) provides the programmer with the capability of reading PROMs and generating critical programming voltages.

The board contains interface buffers, decoding circuitry, miscellaneous control circuitry, digital/analog converters (DACs) for the pin drivers, and power drivers for the programming pins.

The driver board interfaces with the Specific I/O card (702-1835-001) by using hysteresis input buffers. I/O instructions are decoded by two 3-to-8 decoders. The decoder outputs are used to enable reading or writing of various ports. A decoder is used for writing to all DACs. These DACs are for the drivers of pins 1, 20, 21, 22, 23, 26, and 28. There is also a comparison DAC for reading.

These DACs have varying ranges and resolutions for the different drive requirements. Pins 1, 20, 22, and 23 have a resolution of 50 millivolts, as does the comparison DAC. All DACs (except for pin 23 and the comparison DAC) are unipolar and consist of a zero input which corresponds to zero volts out. Pin 23 has an offset so that zero volts out corresponds to a 33 hex input. The comparison DAC ramps from −6.40 to +6.40 volts.

All DAC references are derived from the same 10 volt precision reference.

Other decoder outputs are used for writing to the following registers: LED, address, PROM data, PROM enable, and general purpose control.

The general purpose control register performs the following tasks:

- Three-state and latch control for the data drivers
- Enables pin 1, 22 and 23
- Enables 15 volt supply for VCC drivers
- Beeper control line
- Input and clear or overcurrent memory

The reading of PROM data is a two-step process. In the first step, the appropriate PROM comparator is enabled to allow the reading of data. In the second step, the data is actually read. This same procedure is used to read address

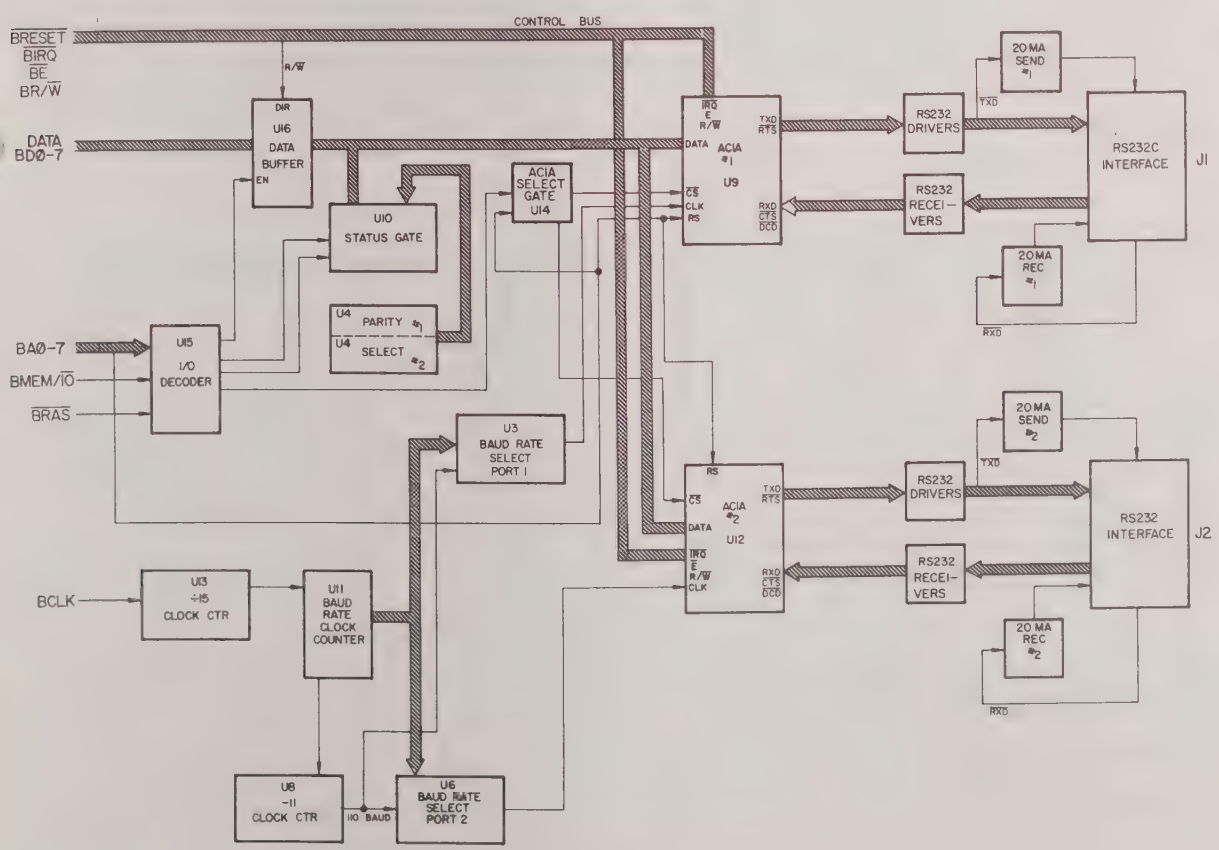


Figure 7-12. Block Diagram, Dual Serial Board

lines and pin drivers. Prior to these steps, the required compare voltage must be written to the comparison DAC. This compare voltage is routed to the minus input on the proper comparator.

7.13 SPECIFIC I/O CARD

Refer to Figure 7-14.

The Specific I/O Card (P/N 702-1835-001) contains interface signal buffers, decoding circuitry, an 8253 interval timer, 16 readable switches and RAM paging control.

A bidirectional buffer is used to supply the data bus to the interface connector. I/O control signals are provided to the interface connector via buffers with hysteresis for noise control. The decoding is done via a 256x4 PROM to allow for different applications.

The 8253 timer counter #0 is driven by the programmer's processor (6809E) clock. Timer counter #0's output drives the clock input of counter #1. Both counter #0 and #1 are enabled simultaneously by executing the appropriate I/O instruction. When counter #1 reaches its terminal count, it generates an interrupt. The interrupt status can be read with the appropriate I/O instruction. This scheme allows one counter to be used as the main counter with the other as a prescaler. Counter #2 is enabled, and its clock input driven, by the output of counter #1.

Two sets of eight switches may be read with the proper instructions. These are general purpose switches.

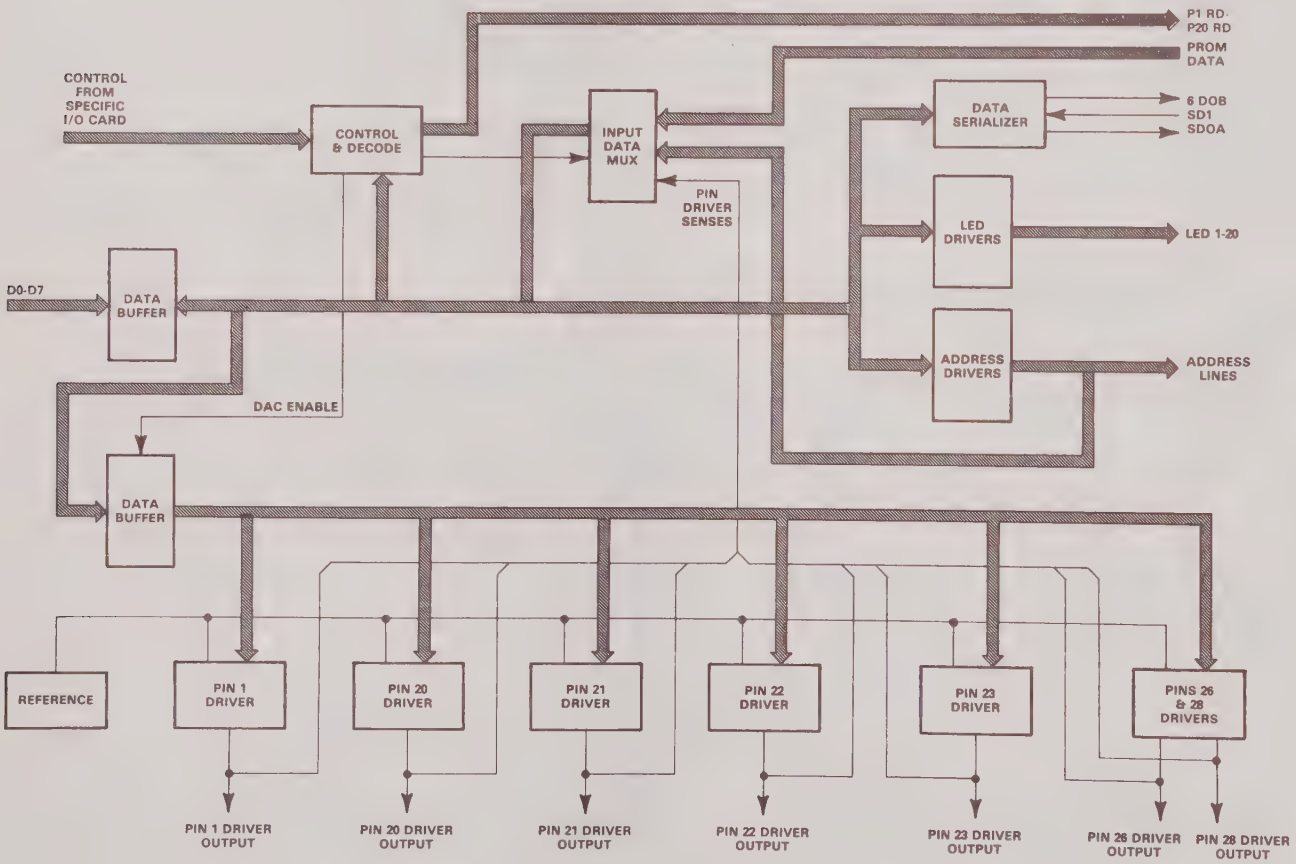


Figure 7-13. Block Diagram, Digital/Analog Driver Board

7.14 SOCKET BOARD

Refer to Figure 7-15.

The Socket Board (P/N 701-1641-001) distributes the various signals to the device sockets. These signals are generated on the Digital/Analog Driver Board (701-1640-001).

Pins 1, 14, 20, 21, 22, 23, 26, and 28 are bused by way of bus bars. These lines are driven from the DAC pin drivers of the driver board (except pin 14 which is ground) by way of a cable assembly.

Address lines A0 through A9, A12 and pin 27 (PGM) are bused on the circuit board since they are low current lines.

Data lines are driven by a CMOS serial-in parallel-out register through 10K resistors. These act as pull-up pull-down isolation resistors for performing device testing (shorts test, backwards device test). The data lines are read through comparators which are enabled for one specific device at a time. The threshold voltage is controlled by the driver board. Device presence is tested by monitoring data line 3 while pulled down to −5 V through a 10K resistor. With the parallel out register loaded with zeros, the 10K resistors act as a divider, bringing data line 3 to −2.5 V when a device is not present.

When a device is installed correctly, data line 3 is pulled up towards ground by using the substrate diode of the device. Diode overvoltage protection on the data lines prevents damage to the data drivers.

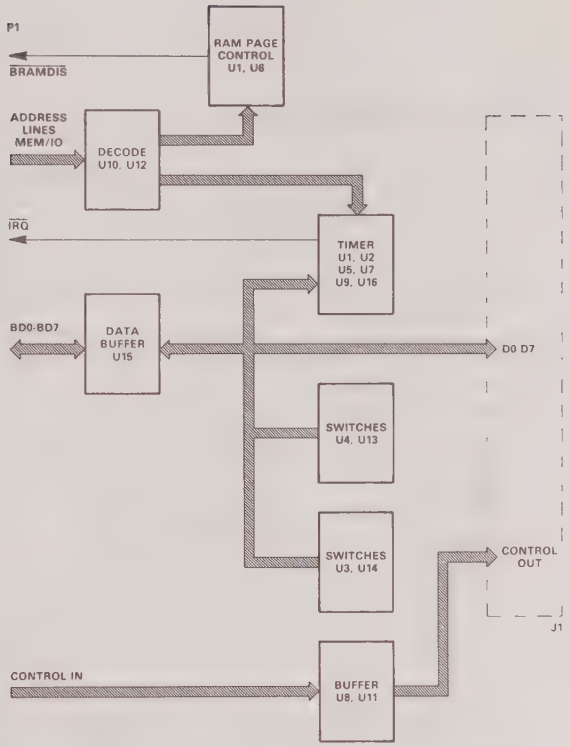


Figure 7-14. Block Diagram, Specific I/O Card

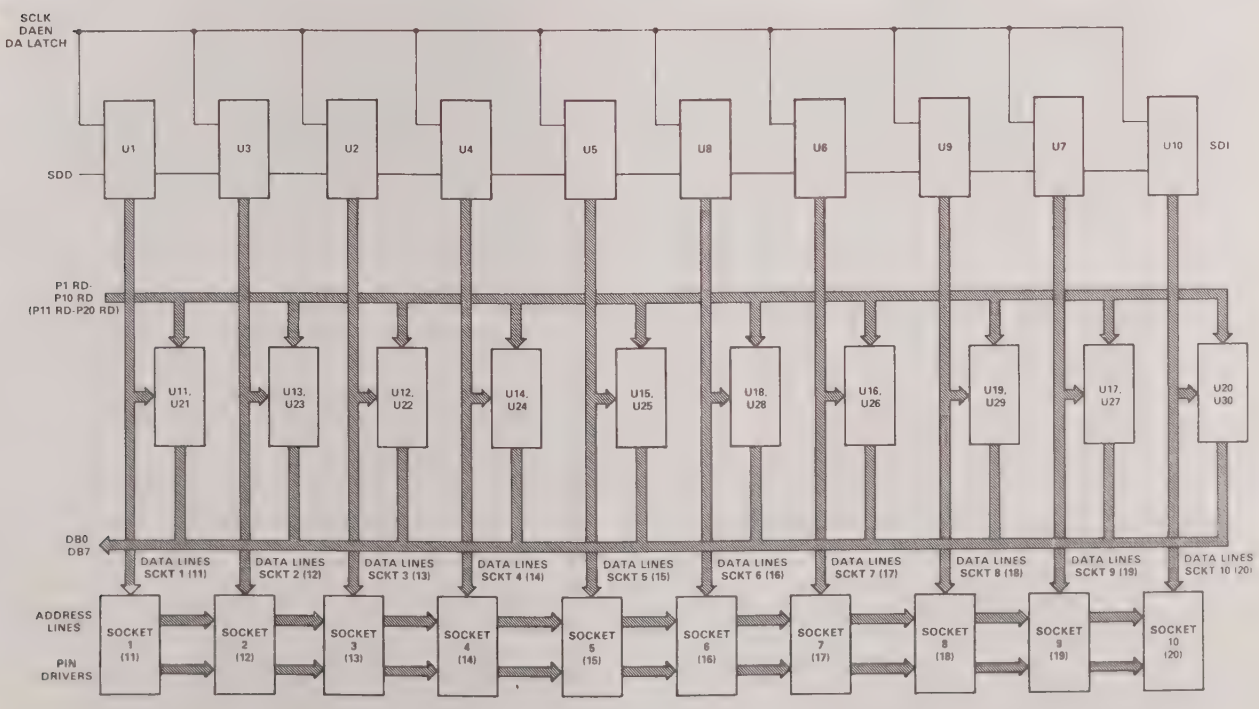


Figure 7-15. Block Diagram, Socket Board

7.15 RAM DISK BOARD

The RAM Disk Board is a sequentially accessed, 128K x 8 dynamic RAM array with controlled interface. It can be broken down into the following blocks.

Interface and control. This block consists of chips U1 and U2. U1 is a programmable logic device which provides the primary decode and control functions for the RAM Disk Board. Table 7-3 lists the U1 functions. U2, 74L5139, provides secondary decode and control functions. Table 7-4 lists the U2 functions.

Table 7-3. U1 Functions

PIN NUMBER	FUNCTION
P23	Data Buffer Enable
P20	$\overline{RAS}$
P14	$\overline{CAS}$ Bank Select
P16	$\overline{CAS}$/Increment Refresh Counter
P17	Counter Enable

Table 7-4. U2 Functions

PIN NUMBER	FUNCTION
P10	Increment Refresh Counter
P11	$\overline{CASA}$
P12	$\overline{CASB}$
P4	Increment Address Counter
P7	Load Address Counter (Low Byte)
P6	Load Address Counter (Mid Byte)
P5	Load Address Counter (Hi Nibble)

Address Generation. Addressing is done by five counters, U4 through U8. Initial address data is loaded into the counters (I/O addresses $84EI, $84E2 and $84E3) in three consecutive operations. One of two I/O addresses, $84E4 and 84E8, is read or written to. Address $84E4 will increment automatically after access is completed and will point to the location in the array for the next reading or writing operation. Address $84E8 does not increment automatically.

Address Multiplexer. The address multiplexer consists of four ICs, U9 through U12. U9 and U10 multiplex the 8-bit $\overline{RAS}$ address and the refresh address. The refresh address will be output anytime that I/O space is not accessed.

The output of U9 and U10 are muxed with the $\overline{CAS}$ address by U11 and U12. When the /E is low, the $\overline{CAS}$ address will be output.

Refresh Counter. U13 is the refresh counter. It provides the refresh address to the address mux and is incremented automatically after each refresh operation.

Dynamic RAM Array. The dynamic RAM array consists of sixteen 4164 (64K x 1 dynamic RAMs) arranged in an array of 128K x 8. The theory of operation for these devices will not be covered here. Please refer to the manufacturers data sheet for descriptions of these devices.

Overall, the RAM Disk Board can operate in the following modes:

- Accessed read with increment
- Accessed read without increment
- Accessed write with increment
- Accessed write without increment
- Non-accessed refresh

Refer to the timing diagram for Family code 93 for detailed timing and operational sequence information.

APPENDIX A
DATA TRANSLATION FORMATS

A.1 INTRODUCTION

This appendix defines the data translation formats available for the 120A/121A. The 120A/121A is capable of interfacing with all RS232C serial equipment employing a data translation format described in this appendix.

Each data translation format is assigned a 2-digit code which the operator enters into the programmer (from the keyboard or, in remote control, through the serial port) to send or receive data in that format. In addition to the data translation format code, there is a 1-digit instrument control code which specifies control characters to be transmitted to, or received from, peripheral instruments.

A.2 DATA VERIFICATION

For data verification the 120A/121A calculates a sum-check of all data sent to or from the programmer. At the end of a successful input operation, the programmer will display the sum-check of all data transferred. It will also compare any received sum-check fields with its own calculation. If the two agree, the programmer will display the sum-check; a mismatch will produce an error message. Output data is always followed by a sum-check field which may be printed on disk or tape for use in subsequent input operations.

A.3 CODES

Each format is assigned a 2-digit data translation format code which the operator enters into the programmer to transfer data in that format. In addition to this code, a 1-digit instrument control code may be used to specify control characters for peripheral equipment. The codes must be formatted as shown in Figure A-1. If no codes are entered into the programmer, the current default values will be in effect.

See Table A-1 for a definition of instrument control codes and Table A-2 for a definition of data translation format codes.

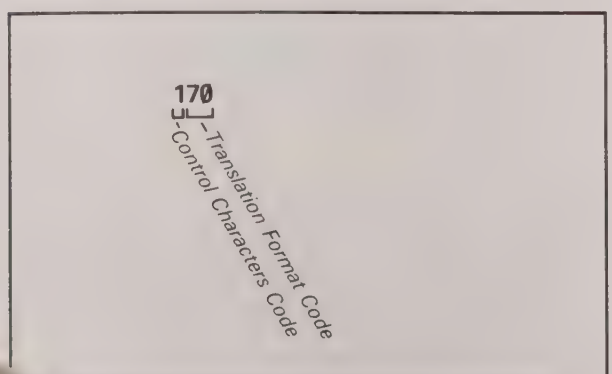


Figure A-1. Formatting the Instrument Control Code and Data Translation Format Code

Table A-1. Instrument Control Codes

CONTROL CODE	PROGRAMMER ACTION
0	No control character sent or acknowledged.
1	Send "reader on" (ASCII DC1/Hex 11) when ready to receive data, and "reader off" (ASCII DC3/Hex 13) when all data is received. Also send "punch on" (ASCII DC2/Hex 12) before sending data, and "punch off" (ASCII DC4/Hex 14) after sending data.
2	Sends data after acknowledging a "reader on" (ASCII DC1/Hex 11), and stops sending data after acknowledging a "reader off" ASCII DC3/Hex 13).

A.4 TRANSLATION FORMATS

This section gives information on the translation formats available for input and output by the 120A/121A.

A.4.1 BINARY TRANSFER, CODE 10

Data transfer in the Binary format consists of a stream of 8-bit data words preceded by a byte count and followed by a sum-check. The Binary format does not have addresses.

A paper tape generated by a programmer will contain a 5-byte, arrow-shaped header followed by a null and a 4-nibble byte count. The start code, a nonprintable rubout in even parity, follows the byte count. The end of data is signalled by 2 nulls and a 2-byte sum-check of the data field. Refer to Figure A-2.

The programmer stores incoming binary data upon receipt of the start character. Data is stored in RAM starting at the first RAM address and ending at the last incoming data byte. Transmission may be aborted by pressing any mode key.

A.4.2 DEC BINARY FORMAT, CODE 11

Data transmission in the DEC Binary format is a stream of 8-bit data words with no control characters except the start code. The start code is one null preceded by at least one rubout. A tape output from the programmer will contain 32 rubouts in the leader. The DEC Binary format does not have addresses.

A.4.3 ASCII BINARY FORMAT, CODES 01, 02 and 03 (or 05, 06, and 07)

In these formats, bytes are recorded in ASCII codes with binary digits represented by N's and P's, L's and H's,

Table A-2. Data Translation Formats

FORMAT	CODE
Binary	10
DEC Binary	11
ASCII-BNPF	01 (05)*
ASCII-BHLF	02 (06)*
ASCII-B1ØF	03 (07)*
Spectrum	12 (13)*
ASCII-Octal (Space)	30 (35) +
ASCII-Octal (Percent)	31 (36) +
ASCII-Octal (Apostrophe)	32
ASCII-Octal SMS	37
ASCII-Hex (Space)	50 (55) +
ASCII-Hex (Percent)	51 (56) +
ASCII-Hex (Apostrophe)	52
ASCII-Hex SMS	57
ASCII-Hex (Comma)	53 (58) +
RCA Cosmac	70
Fairchild Fairbug	80
MOS Technology	81
Motorola Exorciser	82
Intel Intellec 8/MDS	83
Signetics Absolute Object	85
Tektronix Hexadecimal	86
Motorola Exormax	87
Intel MCS-86 Hexadecimal Object	88
Hewlett-Packard 64000 Absolute	89
Texas Instruments SDSMAC	90

* For transmission of data without start codes, these alternate data translation format codes are used.

\+ For transmission of data with the SOH (CTRL A) start code, these alternate data translation format codes are used.

and 1's and 0's, respectively. See Figure A-3. The ASCII Binary formats do not have addresses.

Figure A-3 shows four data byte coded in each of the three ASCII Binary formats. Incoming bytes are stored in RAM sequentially starting at the first RAM address. Bytes are sandwiched between "B" and "F" characters and are normally separated by spaces. Any other characters, such as carriage returns or line feeds, may be inserted between an "F" and the next "B". The start codes are a nonprintable STX, control B (or hex 02 in "no parity"), and the end code is a nonprintable ETX, control C (or a hex 03 in "no parity").

NOTE

Data without a start code may be input to or output from the programmer by use of alternate data translation format codes. These are: ASCII-BHLF, 06; ASCII-B1ØF, 07.

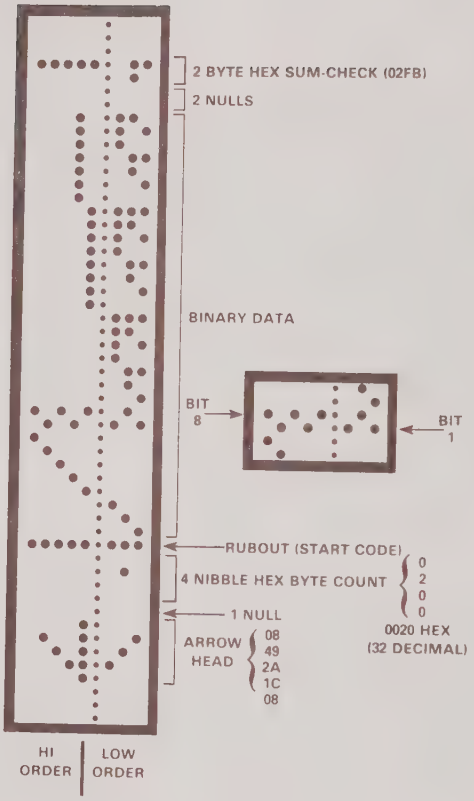


Figure A-2. Input or Output Binary Tape

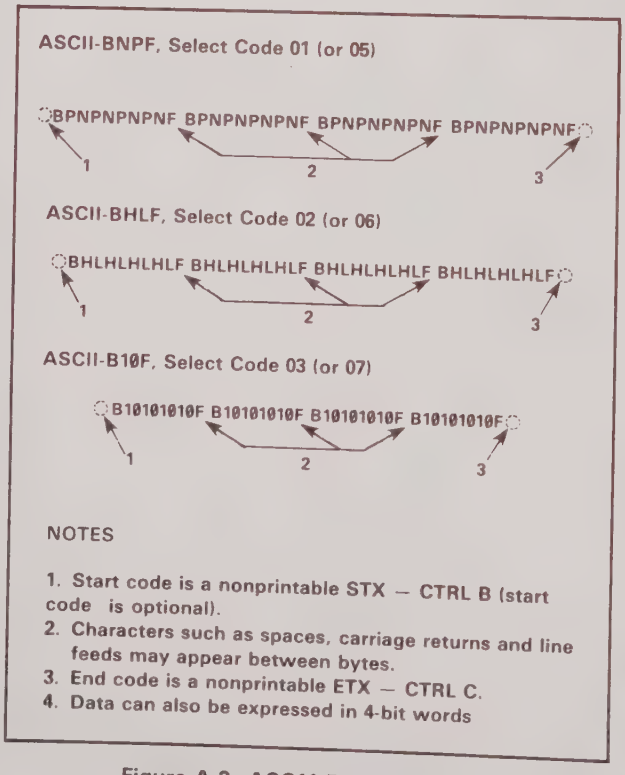

ASCII-BNPF, Select Code 01 (or 05)
BPNPNPNPNF BPNPNPNPNF BPNPNPNPNF BPNPNPNPNF
1
2
3
ASCII-BHLF, Select Code 02 (or 06)
BHLHLHLHLF BHLHLHLHLF BHLHLHLHLF BHLHLHLHLF
1
2
3
ASCII-B1ØF, Select Code 03 (or 07)
B10101010F B10101010F B10101010F B10101010F
1
2
3
NOTES
1. Start code is a nonprintable STX — CTRL B (start code is optional).
2. Characters such as spaces, carriage returns and line feeds may appear between bytes.
3. End code is a nonprintable ETX — CTRL C.
4. Data can also be expressed in 4-bit words

Figure A-3. ASC11 Binary Formats

A single data byte can be aborted if the programmer receives an E character between B and F characters. Data will continue to be stored in sequential RAM addresses. The entire data transfer can be aborted by pressing the key.

Data is output in 4-byte lines with a space between bytes. The transmission is preceded and followed by 50 null characters.

NOTE

Data without a start code may be input to or output from the programmer by use of the alternate data translation format code, 09.

A.4.4 SPECTRUM FORMAT, CODES 12 or 13

In this format, bytes are recorded in ASCII codes with binary digits represented by 1's and 0's. Each byte is preceded by an address.

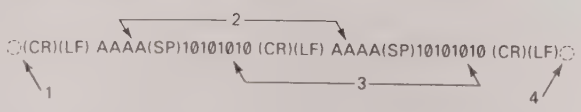
Figure A-4 shows 2 data bytes coded in the Spectrum format. Bytes are sandwiched between the space and carriage-return characters and are normally separated by line feeds. The start code is a nonprintable STX, control B (or hex 02 in "no parity"), and the end code is a nonprintable ETX, control C (or hex 03 in "no parity").

NOTE

Data without a start code may be input to or output from the programmer by use of the alternate data translation format code, 13.

A single data byte can be aborted if the programmer receives an "E" character between a space and a carriage return. Data will continue to be stored in sequential RAM addresses. The entire data transfer can be aborted by pressing any mode key (LOAD, PROG, VERIFY or SELECT).

Data output to a printer will have one address and one byte of data on each line. The programmer first sends an STX (optionally), then the data, and finally an ETX. The transmission is preceded and followed by 50 null characters.



NOTES

1. Start code is a nonprintable STX (start code is optional).
2. Address code is 4 hex digits.
3. 4 or 8 data bits appear between space and carriage return.
4. End code is a nonprintable ETX.

Figure A-4. Spectrum Format

A.4.5 ASCII OCTAL & HEX FORMATS, CODES 30-37 and 50-58

Each of these formats has a start and end code, and similar address and sum-check specifications. Figure A-5 illustrate 4 data bytes coded in each of the 9 ASCII-Octal and Hex Formats. Data in these formats is organized in sequential bytes separated by the execute character (space, percent, apostrophe, or comma). Characters immediately preceding the execute character are interpreted as data. ASCII-Hex and Octal Formats can express 8-bit data, by 2 or 3 octal, or 1 or 2 hex characters. Line feeds, carriage returns and other characters may be included in the data stream as long as a data byte directly precedes each execute character.

Although each data byte has an address, most are implied. Data bytes are addressed sequentially unless an explicit address is included in the data stream. This address is preceded by a "$" and an "A", must contain 2 to 4 hex or 3 to 6 octal characters, and must be followed by a comma, except for the ASCII-Hex (Comma) Format, which uses a period. The programmer skips to the new address to store the next data byte; succeeding bytes are again stored sequentially. See Figure A-6.

Each format has an end code, which terminates input operations. However, if a new start code follows within 16 characters of an end code, input will continue uninterrupted.

NOTE

At least sixteen characters must follow an end code to avoid a timeout error.

After receiving the final end code following an input operation, the programmer calculates a sum-check of all incoming data. Optionally, a sum-check can also be entered in the input data stream. The programmer compares this sum-check with its own calculated sum-check. If they match, the programmer will display the sum-check; if not, a sum-check error will be displayed. Specifications for the optional sum-check are given in Figure A-7.

Output is begun by invoking the Output command. The programmer divides the output data into 8-line blocks.

Data transmission is begun with the start code, a nonprintable STX, optionally SOH.* Data blocks follow, each one prefaced by an address for the first data byte in the block. The end of transmission is signalled by the end code, a nonprintable ETX. Directly following the end code is a sum-check of the transferred data. The transmission is preceded and followed by 50 null characters.

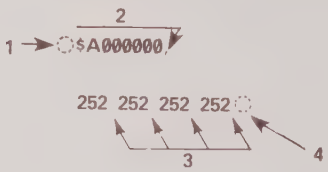
A.4.6 RCA COSMAC FORMAT, CODE 70

Data in this format begins with a start record consisting of the start character (!M or ?M), an address field, and a space. See Figure A-8.

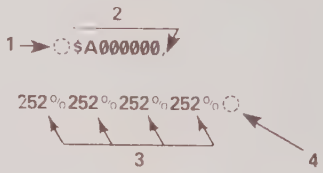
* ASCII-Octal SMS and ASCII-Hex SMS use SOM (CTRL R) as a start code and EOM (CTRL T) as an end code.

The start character ?M is sent to the programmer only by a development system. This happens when the operator enters the interrogation ?M at a terminal (linked in parallel with the programmer to the development system), followed by the address in the development system memory where data transmission is to begin, followed by a number of bytes to be transferred, then by a carriage return. The development system responds by sending ?M to the

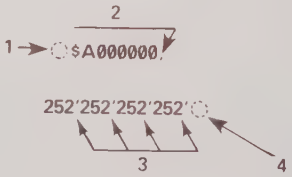
ASCII-Octal (Space), Select Code 30 (or 35)



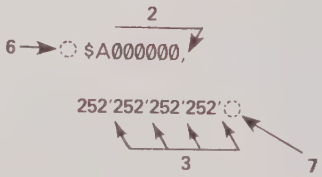
ASCII-Octal (Percent), Select Code 31 (or 36)



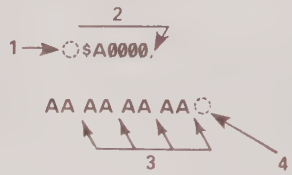
ASCII-Octal (Apostrophe), Select Code 32



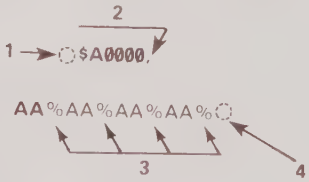
ASCII-Octal SMS, Select Code 37



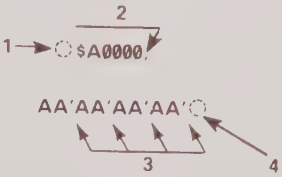
ASCII-Hex (Space), Select Code 50 (or 55)



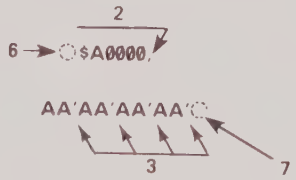
ASCII-Hex (Percent), Select Code 51 (or 56)



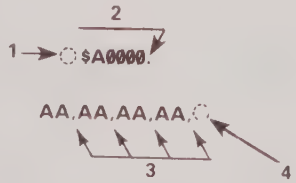
ASCII-Hex (Apostrophe), Select Code 52



ASCII-Hex SMS, Select Code 57



ASCII-Hex (Comma), Select Code 53 (or 58)



NOTES:

1. Start code is nonprintable STX — CTRL B (optionally SOH — CTRL A).
2. Optional address code may precede any data byte. Up to six address digits in octal formats, four in hex.
3. Execute code.
4. End code is a nonprintable ETX — CTRL C.
5. Data can also be expressed in 4-bit form.
6. Start code is nonprintable SOM — CTRL R.
7. End code is a nonprintable EOM — CTRL T.

Figure A-5. ASCII-Octal and Hex Formats

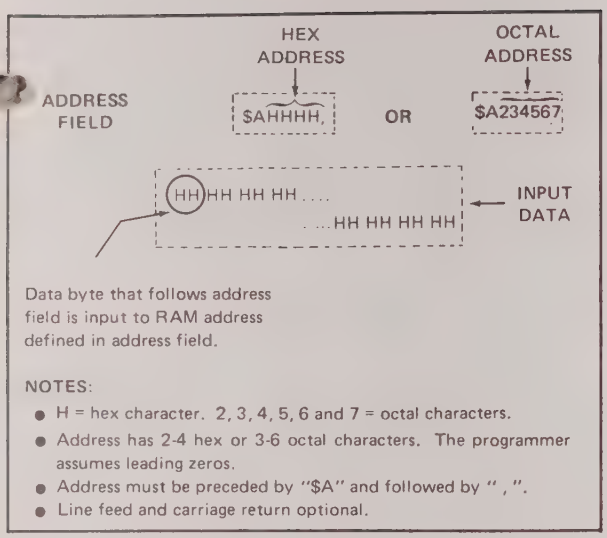

HEX
ADDRESS
OCTAL
ADDRESS
ADDRESS
FIELD
$AHHHH,
OR
$A234567
HH HH HH HH . . . .
. . . .HH HH HH HH
INPUT
DATA
Data byte that follows address
field is input to RAM address
defined in address field.
NOTES:
H = hex character. 2, 3, 4, 5, 6 and 7 = octal characters.
Address has 2-4 hex or 3-6 octal characters. The programmer assumes leading zeros.
Address must be preceded by "$A" and followed by " , ".
Line feed and carriage return optional.

Figure A-6. Optional Address Field in ASCII-Octal and Hex Formats

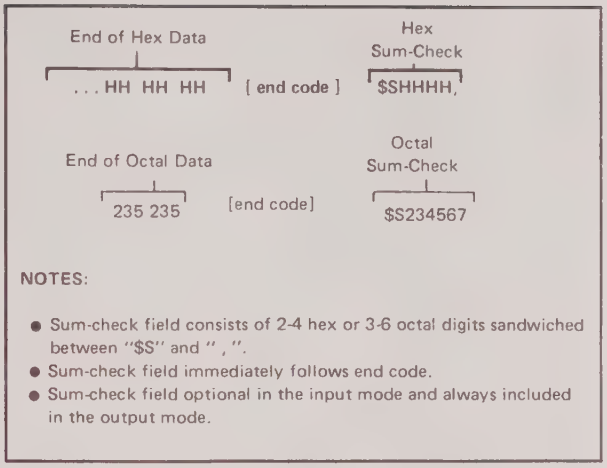

End of Hex Data
. . . HH HH HH
[end code]
Hex
Sum-Check
$SHHHH,
End of Octal Data
235 235
[end code]
Octal
Sum-Check
$S234567
NOTES:
Sum-check field consists of 2-4 hex or 3-6 octal digits sandwiched between "$S" and " , ".
Sum-check field immediately follows end code.
Sum-check field optional in the input mode and always included in the output mode.

Figure A-7. Syntax of the Sum-Check Field in I/O Operations

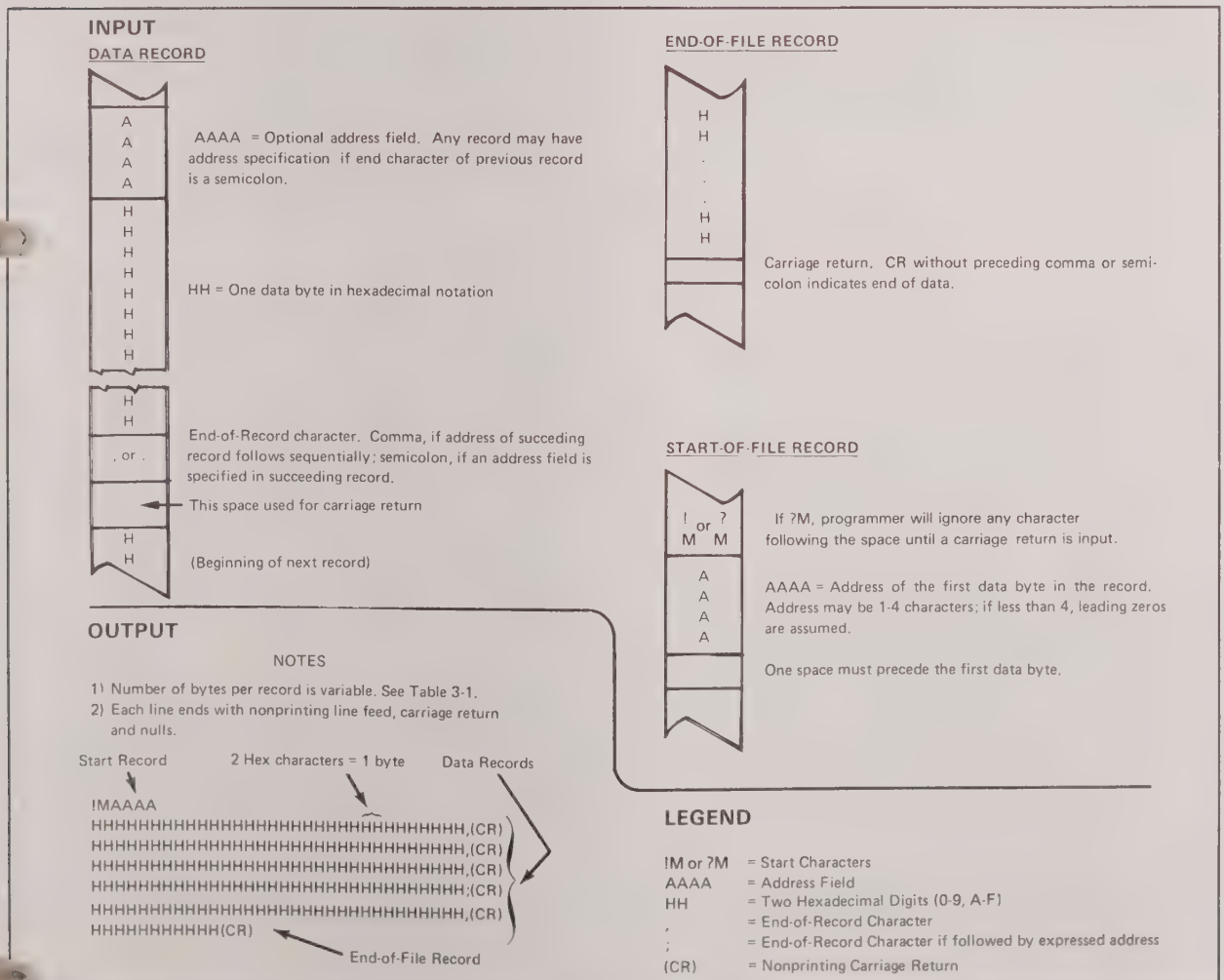


Figure A-8. Specifications for RCA Cosmac Data Files

programmer, followed by the starting address, and a data stream which conforms to the data input format described below. Transmission stops when the specified number of bytes have been transmitted.

Address specification is required for only the first data byte in the transfer. An address must have 1 to 4 hex characters and be followed by a space. The programmer records the next hex character after the space as the start of the first data byte. (A carriage return must follow the space if the start code ?M is used.) Succeeding bytes are recorded sequentially.

Each data record is followed by a comma if the next record is not preceded by an address, or by a semicolon if it starts with an address. Records consist of data bytes expressed as two hexadecimal characters and followed by either a comma or semicolon, and a carriage return. Any characters received between a comma or semicolon and a carriage return will be ignored by the programmer.

The carriage-return character is significant to this format because it can signal either the continuation or the end of data flow; if the carriage return is preceded by a comma or semicolon, more data must follow; the absence of a comma or semicolon before the carriage return indicates the end of transmission.

Output data records are followed by either a comma or a semicolon and a carriage return. The Start-of-File records are expressed exactly as for input. The transmission is preceded and followed by 50 null characters.

A.4.7 MICROPROCESSOR FORMATS

Data in these formats is organized into records characterized by expressed addresses and error-check codes. Each format has record start characters and sum-checks. Records are independent; that is, the programmer can accept addresses in nonsequential order. (The Fairchild Fairbug format differs from the other microprocessor formats in address setting. See the Fairchild Fairbug format description).

• FAIRCHILD FAIRBUG, CODE 80

In the Fairbug format, input and output requirements are identical; both have 8-byte records and identical control characters. Figure A-9 simulates a Fairbug data file. A file begins with a 5-character prefix and ends with a 1-character suffix. The Start-of-File character is an "S", followed by the address of the first data byte. Each data byte is represented by 2 hexadecimal characters.

NOTE

Address specification is optional in this format; a record with no address directly follows the previous record.

A 1-digit hexadecimal checksum follows the data in each data record. The checksum represents, in hexadecimal

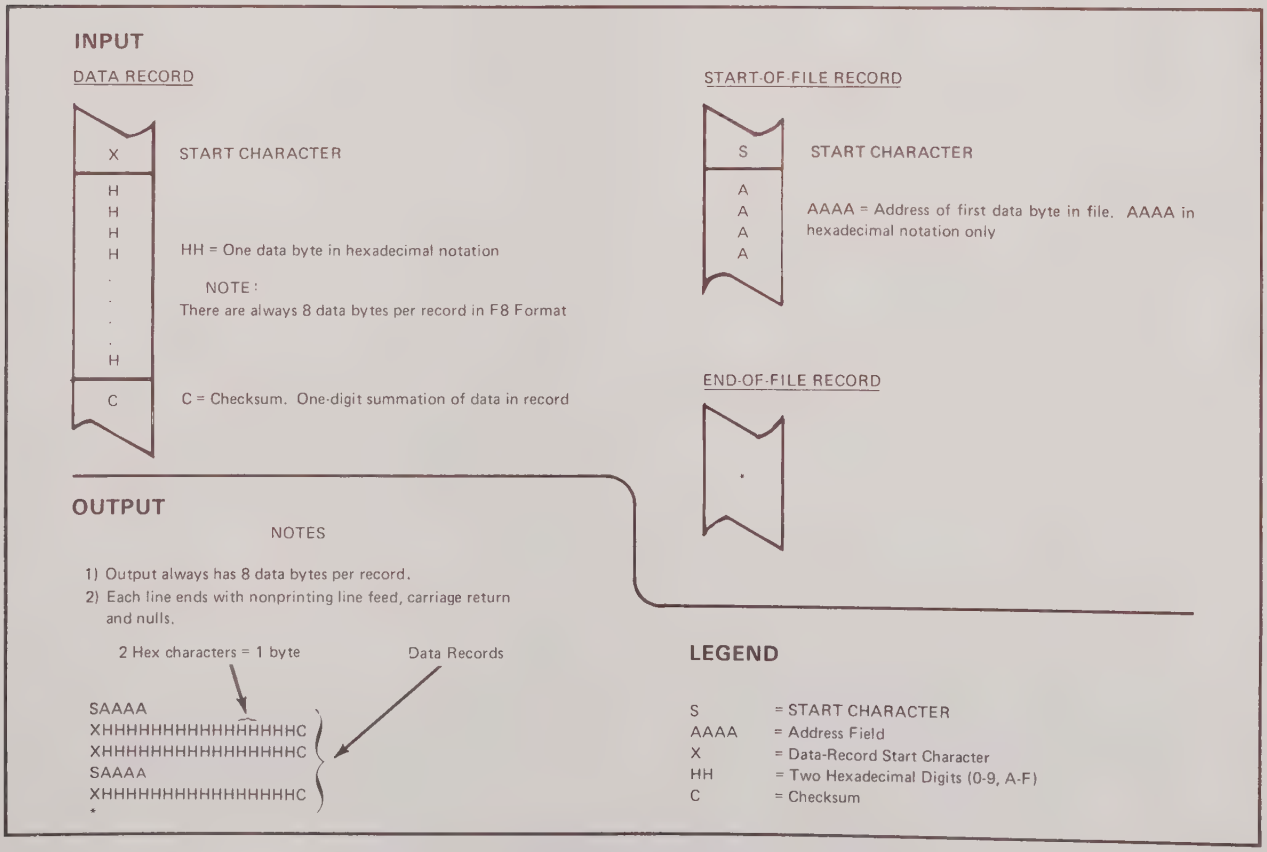


Figure A-9. Specifications for Fairchild Fairbug Data Files

notation, the sum of the binary equivalents of the 16 digits in the record; the half carry from the fourth bit is ignored.

The programmer ignores any character (except for address characters) between a checksum and the start character of the next data record. These spaces can be used for any comments.

The last record consists of an asterisk only, which indicates the end of data transmission.

- **MOS TECHNOLOGY FORMAT, CODE 81**

The data in each record is sandwiched between a 7-character prefix and a 4-character suffix. The number of data bytes in each record must be indicated by the byte count in the prefix. The input file can be divided into records of various length.

Figure A-10 simulates a series of valid data records. Each data record begins with a semicolon. The programmer will ignore all characters received prior to the first semicolon. All other characters in a valid record must be valid hex digits (0-9, A-F). A 2-digit byte count follows the start character. The byte count, expressed in hexadecimal digits, must equal the number of data bytes in the record. The next 4 digits make up the address of the first data byte in the record. Data bytes follow, each represented by 2 hexadecimal digits.

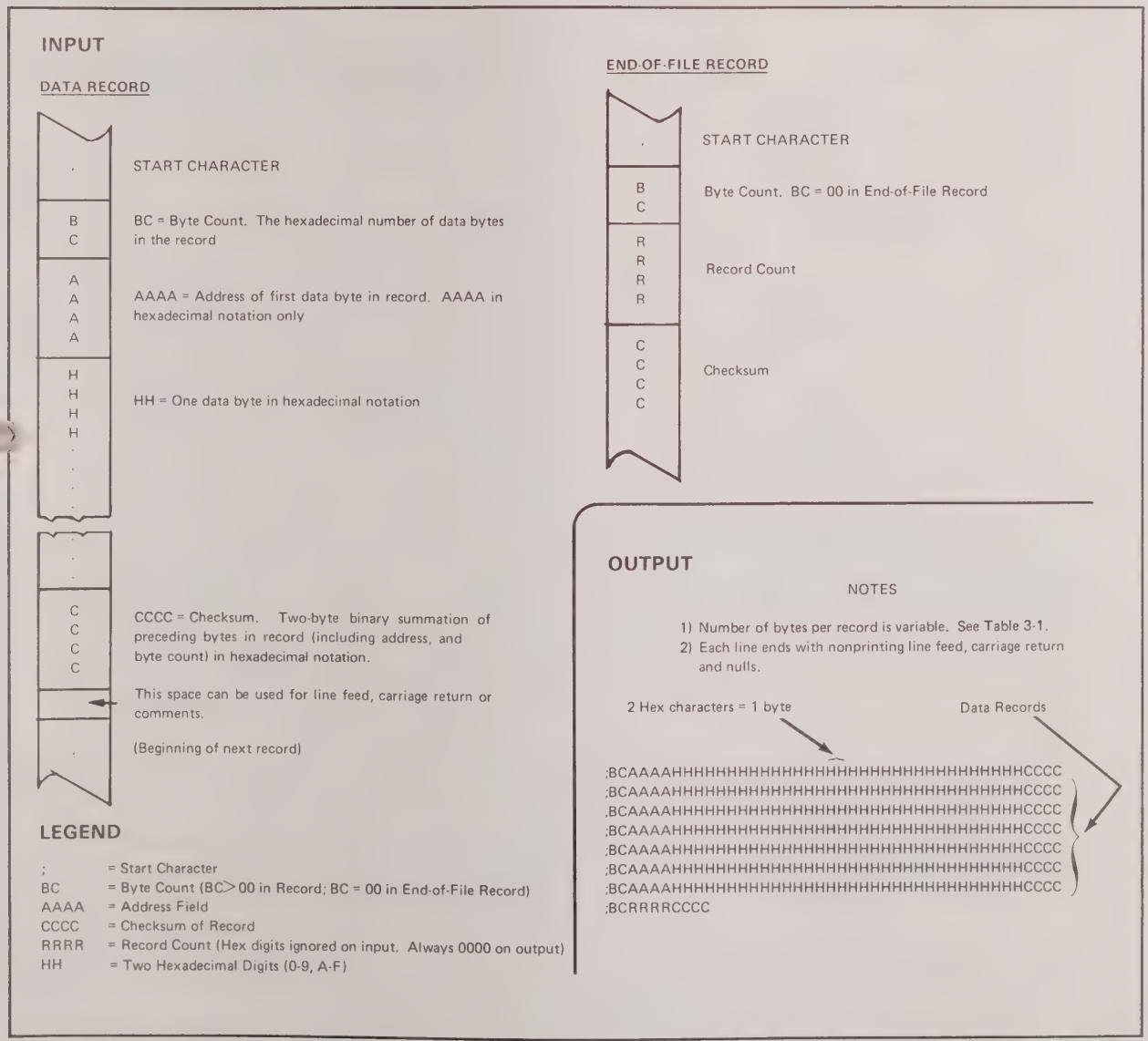


Figure A-10. Specifications for MOS Technology Data Files

• MOTOROLA EXORCISER FORMAT, CODE 82

Motorola data files may begin with a sign-on record, which is initiated by the code S0. Valid data records start with an 8-character prefix and end with a 2-character suffix. Figure A-11 demonstrates a series of valid Motorola data records.

Each data record begins with the start characters "S1"; the programmer will ignore all earlier characters. The third and fourth characters represent the byte count, which expresses the number of data, address and sum-check bytes in the record. The address of the first data byte in the record is expressed by the last 4 characters of the prefix. Data bytes follow, each represented by 2 hexadecimal characters. The number of data bytes occurring must be 3 less than the byte count. The suffix is a 2-character checksum.

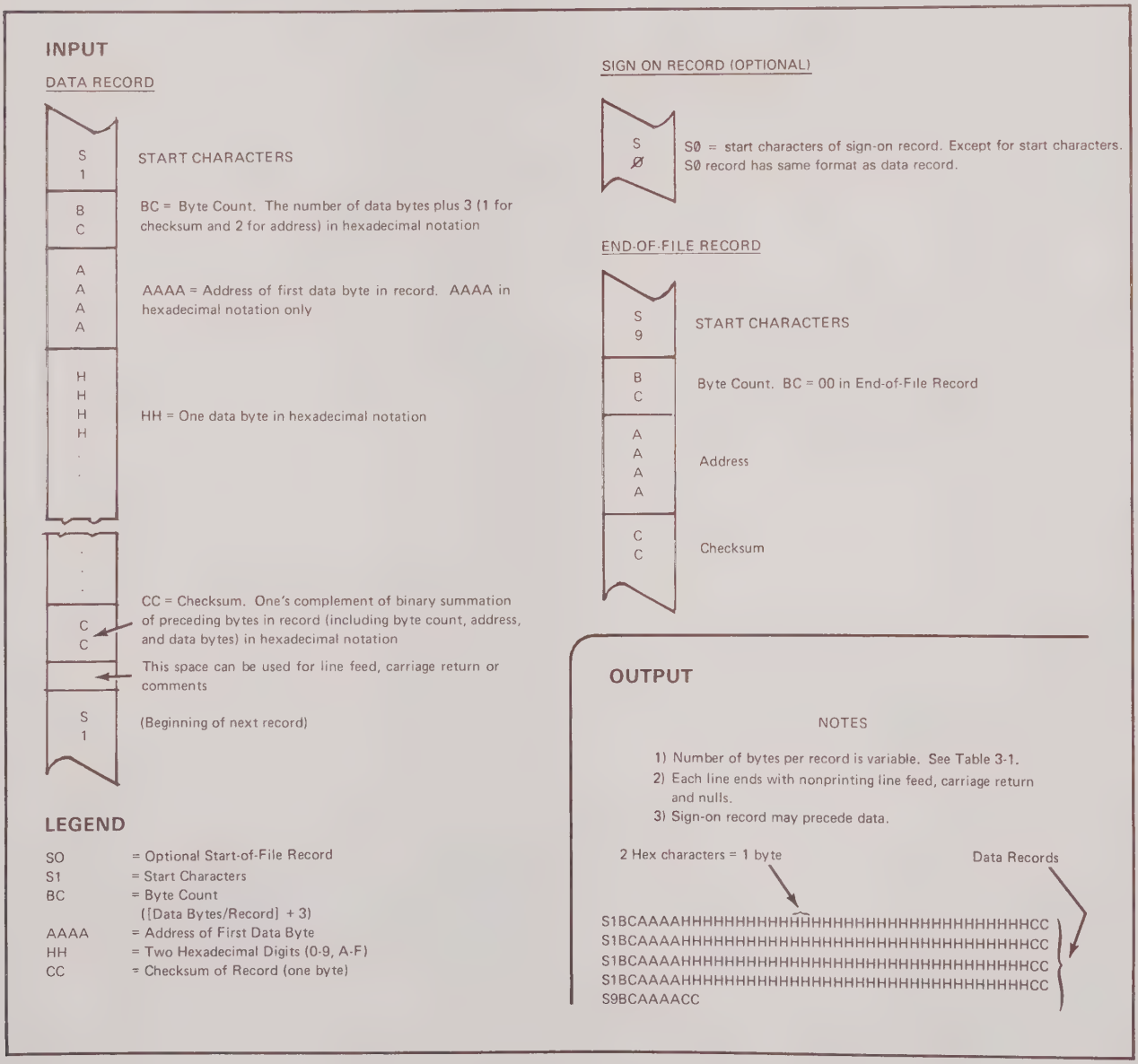

INPUT
DATA RECORD
S 1
START CHARACTERS
B C
BC = Byte Count. The number of data bytes plus 3 (1 for checksum and 2 for address) in hexadecimal notation
A A A A
AAAA = Address of first data byte in record. AAAA in hexadecimal notation only
H H H H . .
HH = One data byte in hexadecimal notation
. . .
C C
CC = Checksum. One's complement of binary summation of preceding bytes in record (including byte count, address, and data bytes) in hexadecimal notation
This space can be used for line feed, carriage return or comments
S 1
(Beginning of next record)
LEGEND
SO = Optional Start-of-File Record
S1 = Start Characters
BC = Byte Count ([Data Bytes/Record] + 3)
AAAA = Address of First Data Byte
HH = Two Hexadecimal Digits (0-9, A-F)
CC = Checksum of Record (one byte)
SIGN ON RECORD (OPTIONAL)
S Ø
SØ = start characters of sign-on record. Except for start characters. SØ record has same format as data record.
END-OF-FILE RECORD
S 9
START CHARACTERS
B C
Byte Count. BC = 00 in End-of-File Record
A A A A
Address
C C
Checksum
OUTPUT
NOTES
1) Number of bytes per record is variable. See Table 3-1.
2) Each line ends with nonprinting line feed, carriage return and nulls.
3) Sign-on record may precede data.
2 Hex characters = 1 byte
Data Records
S1BCAAAAHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHCC
S1BCAAAAHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHCC
S1BCAAAAHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHCC
S1BCAAAAHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHCC
S9BCAAAACC

Figure A-11. Specifications for Motorola Data Files

• INTEL INTELLEC 8/MDS FORMAT, CODE 83

Intel data records begin with a 9-character prefix and end with a 2-character suffix. The byte count must equal the number of data bytes in the record.

Figure A-12 simulates a series of valid data records.

Each record begins with a colon, which is followed by a 2-character byte count. The 4 digits following the byte count give the address of the first data byte.

Each data byte is represented by 2 hex digits; the number of data bytes in each record must equal the byte count.

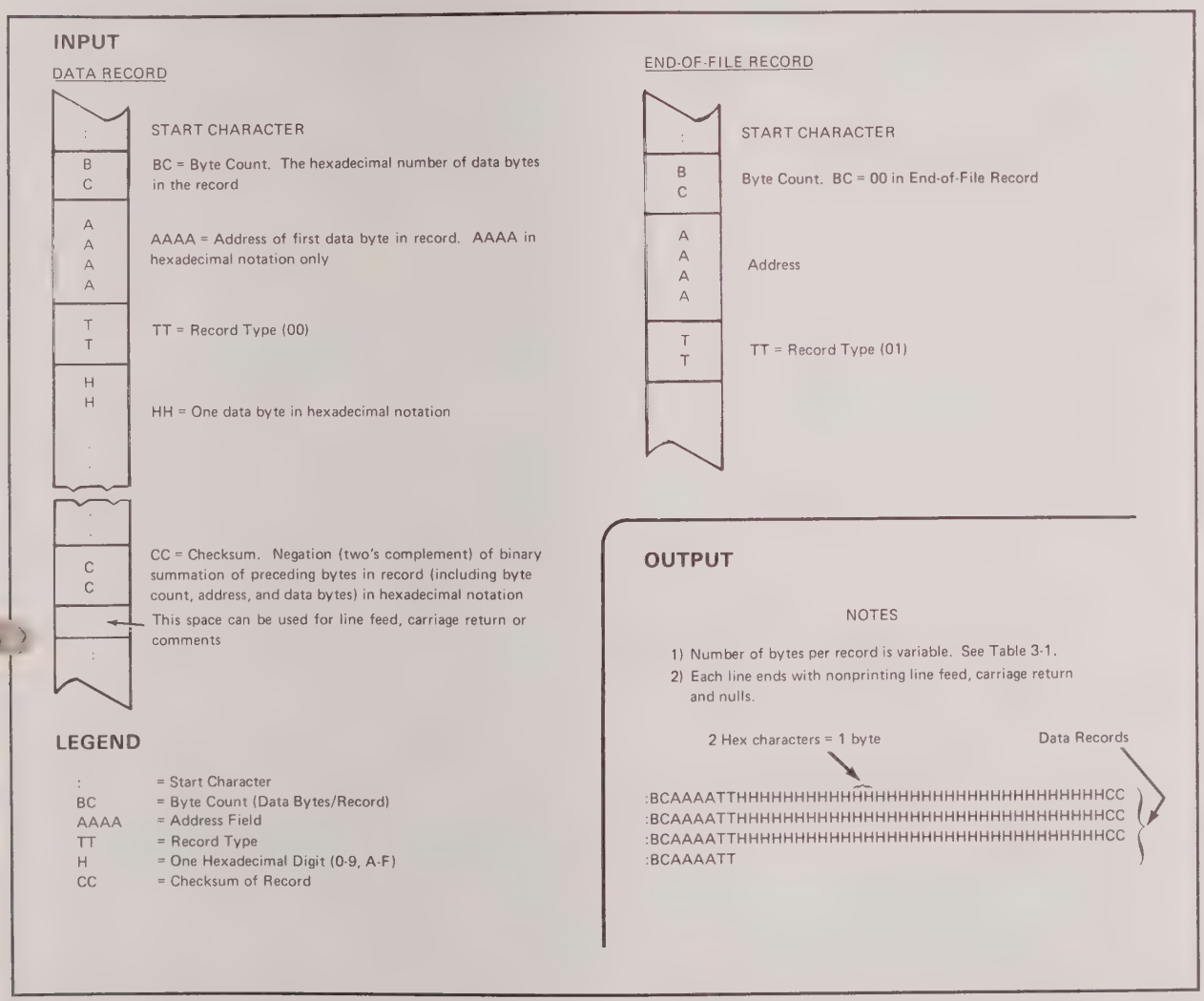

INPUT
DATA RECORD
:
START CHARACTER
B C
BC = Byte Count. The hexadecimal number of data bytes in the record
A A A A
AAAA = Address of first data byte in record. AAAA in hexadecimal notation only
T T
TT = Record Type (00)
H H
HH = One data byte in hexadecimal notation
C C
CC = Checksum. Negation (two's complement) of binary summation of preceding bytes in record (including byte count, address, and data bytes) in hexadecimal notation
This space can be used for line feed, carriage return or comments
END-OF-FILE RECORD
START CHARACTER
Byte Count. BC = 00 in End-of-File Record
Address
TT = Record Type (01)
LEGEND
: = Start Character
BC = Byte Count (Data Bytes/Record)
AAAA = Address Field
TT = Record Type
H = One Hexadecimal Digit (0-9, A-F)
CC = Checksum of Record
OUTPUT
NOTES
1) Number of bytes per record is variable. See Table 3-1.
2) Each line ends with nonprinting line feed, carriage return and nulls.
2 Hex characters = 1 byte
Data Records
:BCAAAATTHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHCC
:BCAAAATTHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHCC
:BCAAAATTHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHCC
:BCAAAATT

Figure A-12. Specifications for Intel Intellec 8/MDS Data Files

• SIGNETICS ABSOLUTE OBJECT FORMAT, CODE 85

Figure A-13 shows the specifications of Signetics format files. The data in each record is sandwiched between a 9-character prefix and a 2-character suffix.

The start character is a colon. This is followed by the address of the first data byte, the byte count, and a 2-digit address check. Data is represented by pairs of hexadecimal characters. The byte count must equal the number of data bytes in the record. The suffix is a 2-character data check, calculated using the same operations described in Figure A-13 for the address check.

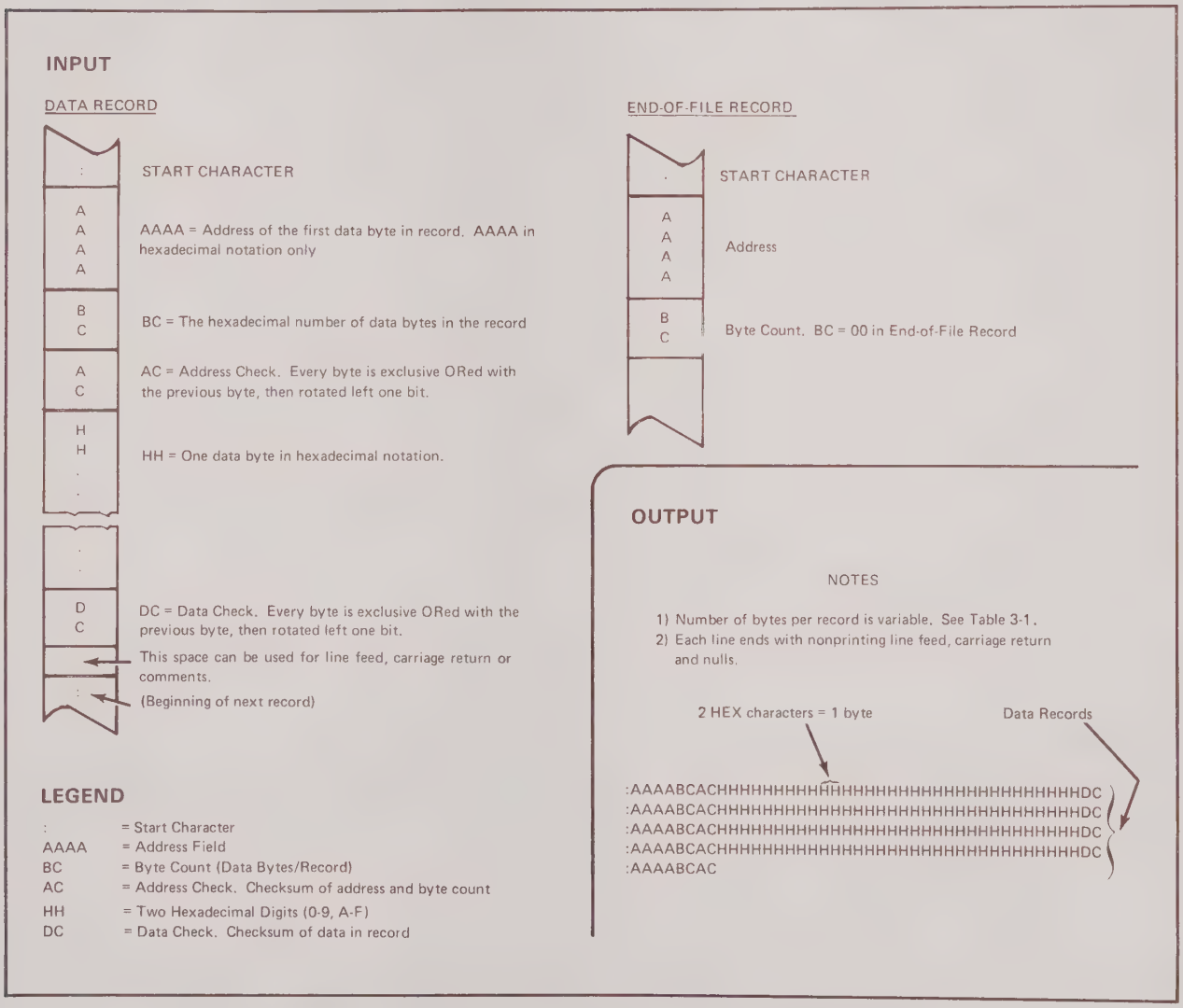

INPUT
DATA RECORD
:
START CHARACTER
A A A A
AAAA = Address of the first data byte in record. AAAA in hexadecimal notation only
B C
BC = The hexadecimal number of data bytes in the record
A C
AC = Address Check. Every byte is exclusive ORed with the previous byte, then rotated left one bit.
H H
HH = One data byte in hexadecimal notation.
D C
DC = Data Check. Every byte is exclusive ORed with the previous byte, then rotated left one bit.
This space can be used for line feed, carriage return or comments.
(Beginning of next record)
END-OF-FILE RECORD
:
START CHARACTER
A A A A
Address
B C
Byte Count. BC = 00 in End-of-File Record
OUTPUT
NOTES
1) Number of bytes per record is variable. See Table 3-1.
2) Each line ends with nonprinting line feed, carriage return and nulls.
2 HEX characters = 1 byte
Data Records
:AAAABCACHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHDC
:AAAABCACHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHDC
:AAAABCACHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHDC
:AAAABCACHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHDC
:AAAABCAC
LEGEND
: = Start Character
AAAA = Address Field
BC = Byte Count (Data Bytes/Record)
AC = Address Check. Checksum of address and byte count
HH = Two Hexadecimal Digits (0-9, A-F)
DC = Data Check. Checksum of data in record

Figure A-13. Specifications for Signetics Absolute Object Data Files

• TEKTRONIX HEXADECIMAL FORMAT, CODE 86

Figure A-14 illustrates a valid Tektronix data file. The data in each record is sandwiched between the start character (a slash) and a 2-character sum-check. Following the start character, the next 4 characters of the prefix express the address of the first data byte. The address is followed by a byte count, which represents the number of data bytes in the record, and by a sum-check of the address and byte count. Data bytes follow, represented by pairs of hexadecimal characters and succeeded by a sum-check of the data bytes. The End-of-File record consists only of control characters used to signal the end of transmission and a byte count and sum-check for verification.

Data is output from the programmer starting at the first RAM address and continuing until the number of bytes in the specified block has been transmitted. The programmer divides output data into records prefaced by a start character and an address field for the first byte in the record. The transmission is preceded and followed by 50 null characters.

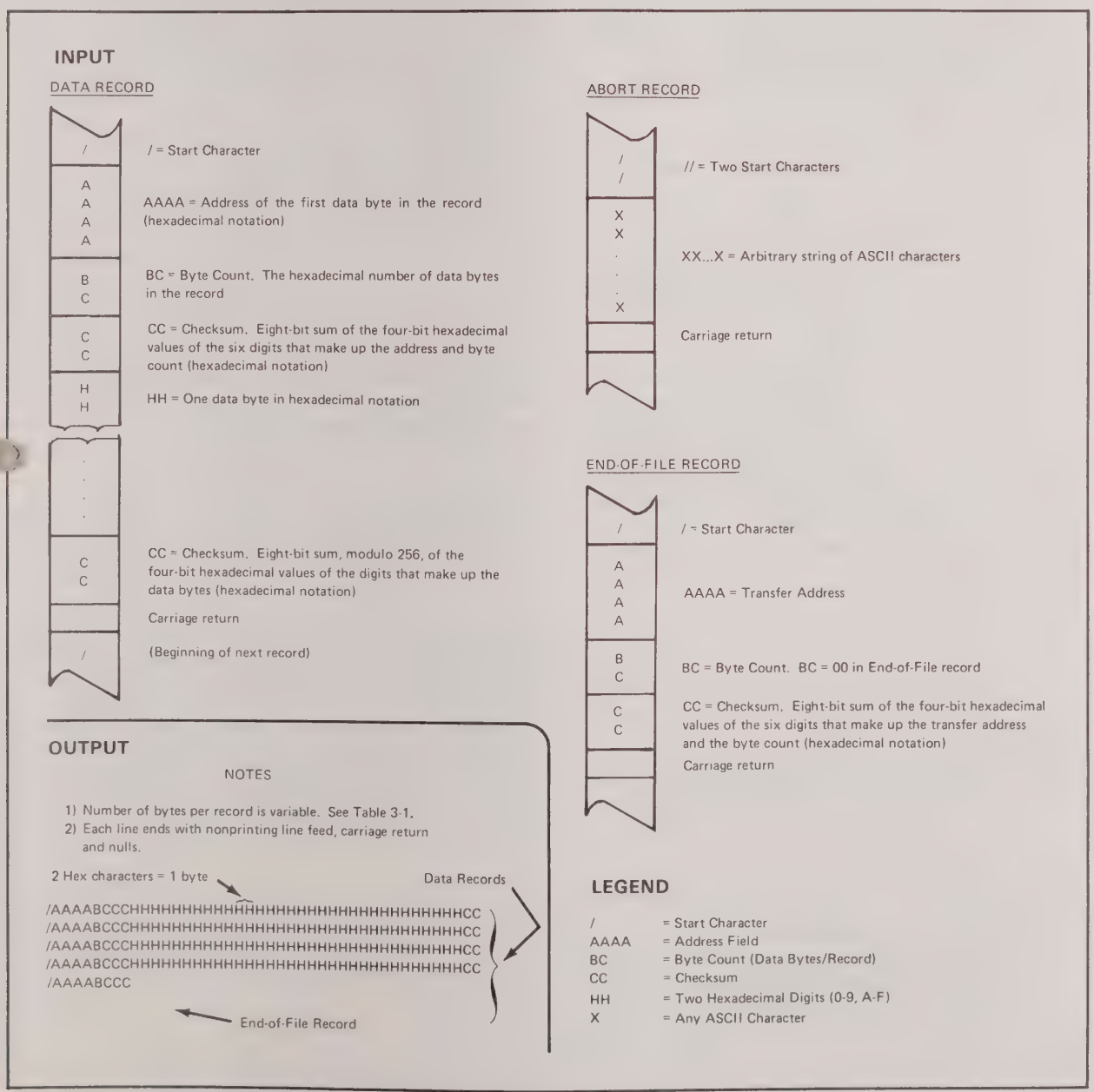


Figure A-14. Specifications for Tektronix Hexadecimal Data Files

• MOTOROLA EXORMAX FORMAT, CODE 87

Motorola data files may begin with a sign-on record, initiated by the code S0. Data records start with an 8- or 10-character prefix and end with a 2-character suffix. Figure A-15 demonstrates a series of Motorola Exormax data records.

Each data record begins with the start characters S1 or S2—S1 if the following address field has 4 characters, S2 if it has 6 characters. The third and fourth characters represent the byte count, which expresses the number of data, address and checksum bytes in the record. The address of the first data byte in the record is expressed by the last 4 characters of the prefix (6 characters for addresses above hex FFFF). Data bytes follow, each represented by two hexadecimal characters. The number of data bytes occurring must be 3 less than the byte count. The suffix is a 2-character checksum.

• HEWLETT-PACKARD 64000 ABSOLUTE FORMAT, CODE 89

Hewlett-Packard Absolute is a binary format with control and data-checking characters. See Figure A-16.

Data files begin with a Start-of-File record including the data bus width, data width base, transfer address, and a checksum of the bytes in the record.

Data records follow the Start-of-File record. Each begins with 2 byte counts: the first expresses the number of 16-bit words in the record not including the checksum and itself; the second expresses the number of 8-bit data bytes in the record. Next comes a 32-bit address which describes the storage location of the following data byte. Data bytes follow; after the last data byte comes a checksum of every byte in the record except the first byte.

The End-of-File record consists only of a byte count, which is always zero.

• TEXAS INSTRUMENTS SDSMAC FORMAT, CODE 90

Data files in the SDSMAC format consist of a Start-of-File record, data records, and an End-of-File record. See Figure A-17.

Each record is composed of a series of small fields, each initiated by a tag character. The programmer recognizes and acknowledges the following tag characters:

Ø - always followed by a file header.

7 - always followed by a checksum which the programmer acknowledges.

8 - always followed by a checksum which the programmer ignores.

9 - always followed by a load address.

B - always followed by 4 data characters.

F - denotes the end of a data record.

The Start-of-File record begins with a tag character and a 12-character file header. Next come interspersed address fields and data fields (each with tag characters). If any data fields appear before the first address field in the file, the first of those data fields is assigned to address ØØØØ. Address fields may be expressed for any data byte, but none are required. The record ends with a checksum field initiated by the tag character 7 or 8, a 4-character checksum, and the tag character F.

Data records follow the same format as the Start-of-File record but do not contain a file header.

The End-of-File record consists of a colon (:) only. The output translator sends a control S after the colon.

•INTEL MCS-86 HEXADECIMAL OBJECT, CODE 88

The Intel 16-Bit Hexadecimal Object file record format is basically the same as the Intel Intellec 8/MDS (Code 83). It starts with nine characters (four fields) that define the start of record, byte count, load address, and record type. It ends with a 2-character checksum. Figure A-12 (Intel Intellec 8/MDS) illustrates this format.

There are four record types:

Ø = data record
Ø1 = end record (signals end of file)
Ø2 = extended address record (added to the offset to determine the absolute destination address)
Ø3 = start record (ignored)

Record type Ø2, the extended address record, defines bits 4 to 19 of the segment base address. It can appear randomly anywhere within the object file and in any order; *i.e.,* it can be defined such that the data bytes at high addresses are sent before the bytes at lower addresses. Because the data bytes are sent in nonsequential fashion, the address offset must be entered into the programmer every time the data transfer is initiated. It is the same as a data record with only four data digits. It's address field is always ØØØØ.

NOTE

Aways specify the address offset when using this format, even when the offset is zero.

INPUT

DATA RECORD

S 1 or S 2	START CHARACTERS. S1 if following address field has 4 characters; S2 if address field has 6 characters.
B C	BC = Byte Count. The number of data bytes plus 3 (1 for checksum and 2 for address) in hexadecimal notation.
A A A A A A	AAAA or AAAAAA = Hexadecimal address of first data byte in record.
H H H H . . .	HH = One data byte in hexadecimal notation.
. . .	
C C	CC = Checksum. One's complement of binary summation of preceding bytes in record (including byte count, address, and data bytes) in hexadecimal notation.
	This space can be used for line feed, carriage return or comments. The programmer will ignore any characters inserted between the last checksum and the start characters of the next record.
S 1 or S 2	(Beginning of next record)

SIGN-ON RECORD (OPTIONAL)

S Ø	SØ = Start characters of sign-on record. Except for start characters SØ record has same format as data record.

END-OF-FILE RECORD

S 8 or S 9	START CHARACTERS. Must be S9 if previous data record began with S1. May be S8 or S9 if previous record began with S2.
B C	Byte Count. BC = 03 in End-of-File Record.
A A A A	Address. Always ØØØØ in End-of-File Record.
C C	Checksum

LEGEND

SO	=	Optional Record Start Characters
S1	=	Start Characters
BC	=	Byte Count ([Data Bytes/Record] +3)
AAAA AAAAAA	=	Address of First Data Byte
HH	=	Two Hexadecimal Digits (0-9, A-F)
CC	=	Checksum of Record (one byte)

OUTPUT

NOTES

1) Number of bytes per record is variable.
2) Each line ends with nonprinting line feed, carriage return and nulls.
3) Sign-on record may precede data.

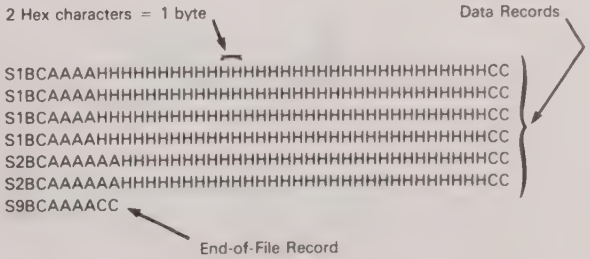


Figure A-15. Specifications for Motorola Exormax Data Files

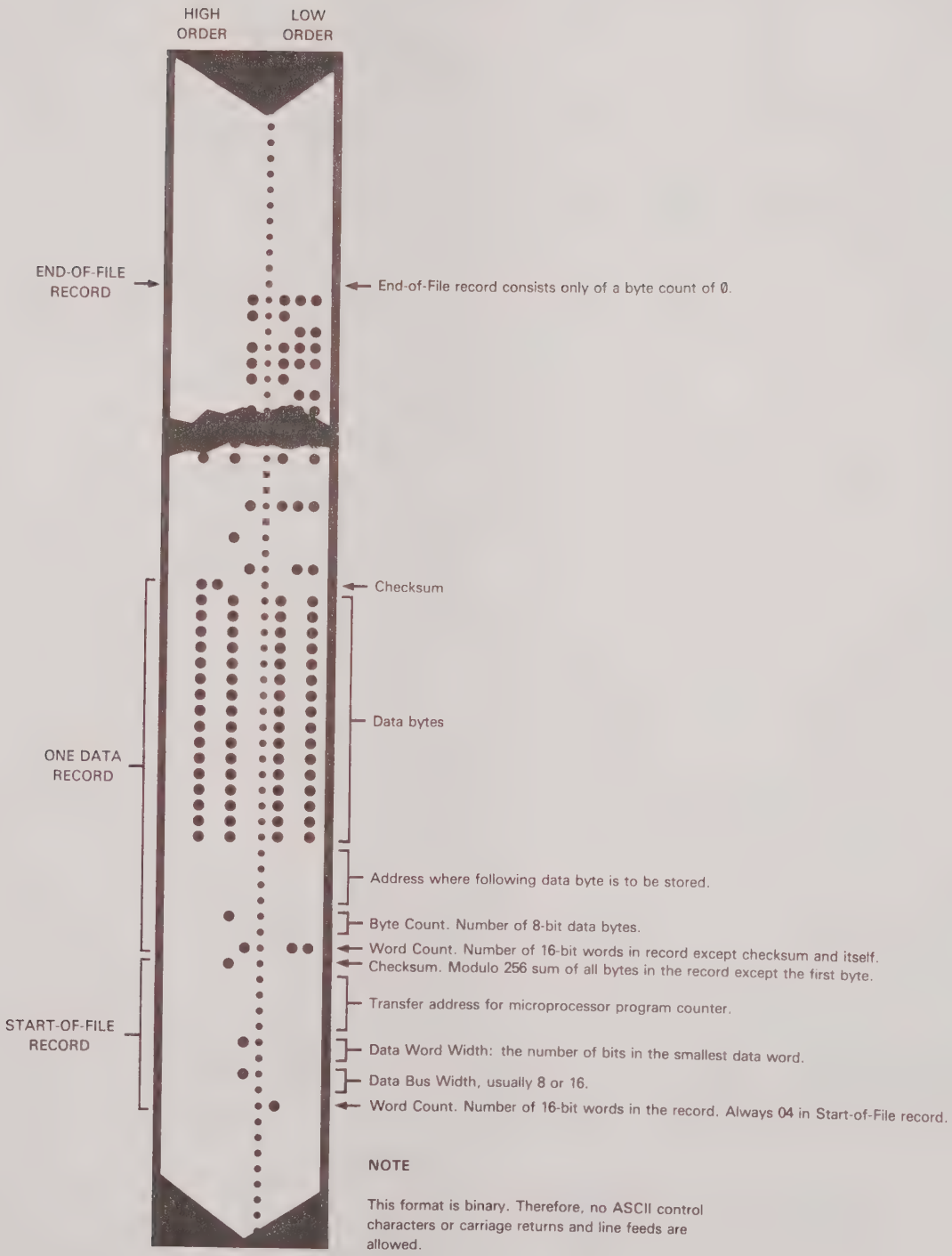

HIGH ORDER
LOW ORDER
END-OF-FILE RECORD
End-of-File record consists only of a byte count of Ø.
Checksum
Data bytes
ONE DATA RECORD
Address where following data byte is to be stored.
Byte Count. Number of 8-bit data bytes.
Word Count. Number of 16-bit words in record except checksum and itself.
Checksum. Modulo 256 sum of all bytes in the record except the first byte.
Transfer address for microprocessor program counter.
START-OF-FILE RECORD
Data Word Width: the number of bits in the smallest data word.
Data Bus Width, usually 8 or 16.
Word Count. Number of 16-bit words in the record. Always 04 in Start-of-File record.
NOTE
This format is binary. Therefore, no ASCII control characters or carriage returns and line feeds are allowed.

Figure A-16. Specifications for Hewlett Packard Absolute Format Data Files

INPUT

START-OF-FILE RECORD

Ø	Tag Character. Always followed by a file header.
X X X X Y Y Y Y Y Y Y Y	File Header. XXXX = hexadecimal byte count of 16-bit data bytes in the record. YYYYYYYY = name of file. May be any ASCII character in hexadecimal notation.
9	Optional Tag Character. Always followed by a load address. Tag characters 9 and B may come in any order.
A A A A	Load Address: 4-character hexadecimal address of first data byte in the record.
B	Tag Character. A "B" must precede every 4 data characters.
H H H H	HH = 2-character hexadecimal data byte.
B	
H H H H	
7 or 8	Tag Character. Must be followed by a 4-character checksum field. If 8, programmer will ignore the checksum.
C C C C	Hexadecimal Checksum. Two's complement of the sum of the 8-bit ASCII values of the characters in the record from the first tag character through the checksum tag (7 or 8).
F	Tag Character. Denotes end of the data record. All characters following F before line feed and carriage return will be ignored.

DATA RECORD

9	Optional Tag Character. Always followed by a load address. Tag characters 9 and B may come in any order.
A A A A	AAAA = Load address: 4-character hexadecimal address of first data byte in the record.
B	Tag Character. A "B" must precede every 16-bit data byte.
H H H H	HH = 2-character hexadecimal data byte.
B	
H H H H	
B	
H H H H	
7 or 8	Tag Character. Must be followed by a 4-character checksum field. If 8, checksum will be ignored by programmer.
C C C C	Checksum in hexadecimal notation. Two's complement of the sum of the 8-bit ASCII values of the characters in the record from the first tag character through the checksum tag (7 or 8).
F	Tag character. Denotes end of data record. All characters following F before line feed and carriage return will be ignored.

END-OF-FILE RECORD

LEGEND

Ø,7,8,9,B,F = Tag Characters
AAAA = Address Field
XXXX = Byte Count
YYYYYYYY = File Name
HH = Two Hexadecimal Digits (0-9, A-F)
CCCC = Checksum

OUTPUT

NOTES

1)Number of bytes per record is variable.
2)Each line ends with nonprinting line feed, carriage return and nulls.

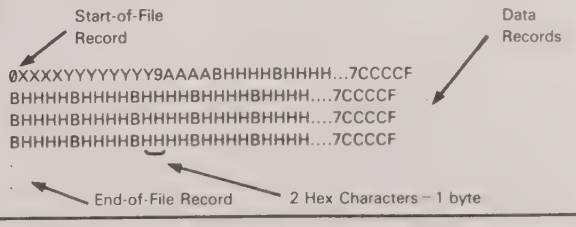


Figure A-17. Specifications for Texas Instruments SDSMAC Data Files

APPENDIX B
REFERENCE MATERIAL

Table B-1. Glossary
Table B-2. Abbreviations
Table B-3. Cross-Reference Chart of Number Bases
Table B-4. ASCII and IEEE Code Chart
Table B-5. ASCII Control Characters

Table B-1. Glossary

address field. Optional set of control characters in a data translation format. It defines the address of the next data byte.

address offset. A 4-digit hex value subtracted from addresses on input and then added to addresses output from the programmer. The result is added to the begin device address or begin RAM address as applicable.

begin device address. The first device address from which or to which data is being transferred.

begin RAM address. The first address of the programmer data RAM from which or to which data is to be transferred.

blank check. A test performed by a programmer to detect the presence of any programmed bits. A device with no programmed bits is "blank."

block size. The hexadecimal number of bytes to be transferred in a data transfer.

bootstrap. The basic software routine which performs initial power-up machine checks and prepares the machine to receive and respond to operating system instructions.

configuration number. A 4-digit hex number that identifies the software revision level of the programmer.

data translation format. Form in which the translator software accepts input data. Also the form for data output by the unit.

default value. The value the unit uses for a parameter unless the operator specifies another value.

device. Any PROM, EPROM, MOS PROM, or programmable logic array.

end code. Character in a data translation format which signals the completion of a data transfer.

error code. A code which signals specific errors to the operator.

Family and Pinout Codes. Two-digit codes used by some Data I/O programming modules to identify programming variables including pinout, address limit and programming algorithms.

FIP. Flourescent Indicator Panel.

generic family. Devices of different memory size developed by a manufacturer that require the same programming voltages, currents, and timing relationships. They can be programmed by the same programming module.

handshaking. The required sequence of signals for communication between two units. The I/O bus protocol for a unit defines its handshaking requirements. This is especially true for asynchronous I/O systems in which each signal requires a response to complete an I/O operation.

illegal-bit test. A test performed by a programmer to detect the presence of any programmed bits of incorrect polarity (illegal bits).

mode. A software routine in a machine, characterized by a specific automatic sequence of steps.

nibble. One half of an 8-bit byte.

programming module. Generic term for Data I/O Programming Pak, Program Card Set, UniPak, Gang Module, FPLF Pak, MOS Pak, IFL Pak, and other programming electronics.

record size. The number of bytes printed on a line of a teletype or other printer; or the number of bytes printed on a paper tape before another address field is printed.

scratch pad memory. The internal memory used for performing calculations.

select function. A 2-digit hex number used to specify data translation formats, serial interface operations, or certain RAM data manipulations.

start code. Character in a data translation format which signals the beginning of a data transfer.

sum-check. A summation of bits calculated according to the rules of simple addition and usually expressed as a 4-digit hex number; any carry from the most significant bit or digit is discarded. A sum-check is used to verify the integrity of data transfers.

When the sum-check is displayed after a program operation it will appear in either of two ways:

S*-XXXX Sum of all bytes in an operation.

SC-XXXX Sum of bytes in a block of data. A block is defined as the block size when it is greater than the word-limit. When sets are being programmed, a block is defined as the word-limit times the number of devices in the set.

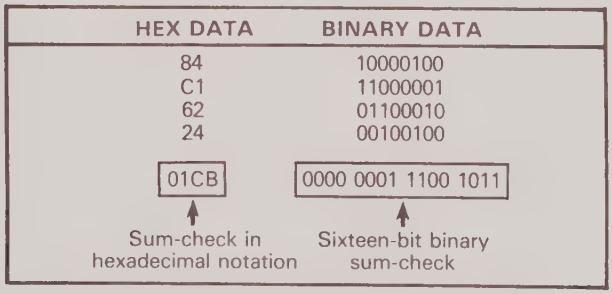


Figure B-1. Sample Sum-check Calculation

waveforms (programmable). The graphical representation of the timing and magnitude of programming pulses. If the programming waveforms are not kept within tolerance, programming yield is jeopardized.

word limit. The highest address in a device. For example, the word limit of a 1Kx8 device is 1K (or hex 3FF). Synonymous with address limit.

word width. The number of bits in a byte or word (4 or 8).

Table B-2. Abbreviations

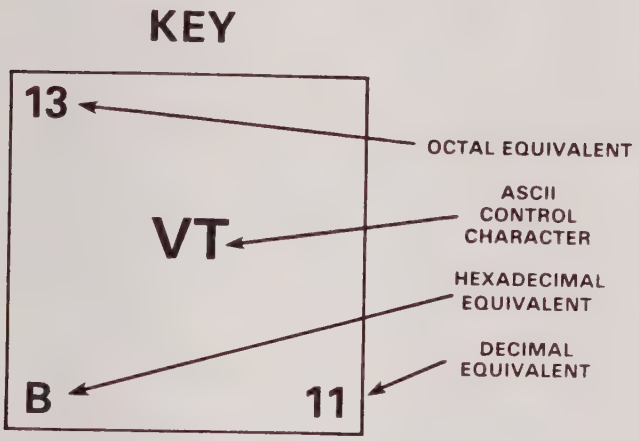
The following is a list of abbreviations commonly used in Data I/O Instruction manuals.

A_4 - address line 4
ADDR - address
BC - bin count, number of bins
BR - bridge rectifier
C - capacitor
Clk - clock
Clk. Inh. - clock inhibit
Cntl. - control
Cont. - control
CR - diode
CTS - Clear To Send
D_5 - data line 5
DAC - Digital to Analog Converter
DC - division count, number of partitions
DCD - Data Carrier Detect
DCU - Data I/O Data Control Unit
DI_2 - data input 2
DIR - Directory
DO_2 - data output 2
DS - display
DSR - Data Set Ready
DTR - Data Terminal Ready
DVM - digital voltmeter
Emul - emulate
ERR - error
ESC - escape
F - fuse
FC - Translation Format Code
FFPP - Family Code (FF) and Pinout Code (PP)
FRME - frame
Fwd. - Forward
Gnd. - Ground
HLT. - Halt
HV - high voltage
ID_4 - identification line 4
I/O - Input/Output
IRQ - Interrupt Request
J - jack or connector
JP - jumper
K - relay
LIM - limit
LSB - Least Significant Bit
LSD - Least Significant Digit
MSB - Most Significant Bit
MSD - Most Significant Digit
NMI - Non-Maskable Interrupt
NO CONT SECT - No Contiguous Sector
Oper. - operate
PA_{15} - programmer address line 15
PAK - programming module
PCS - Program Card Set
PD_6 - programmer data line 6
PN - Part Number
Prog - Program
Prog. Pulse - Program Pulse
PROM - Programmable Read Only Memory
Q - transistor
R - resistor
RAM - Random Access Memory
Read Inh. - Read Inhibit
Rec. - receive
Rev. - reverse
RP - resistor pack
RST - Reset
R/W - Read/Write
RX - Receive Data
S - switch
TOR - Turn On Reset
TX - Transmit Data
U - integrated circuit device
V•02 - the "AND"-ing of the Valid Memory Address line and the phase 2 line
Ver. A - Verify pass A
Ver. B - Verify pass B
VFY - verify
VMA - Valid Memory Address
VR - Voltage Regulator
V_{REF} - Voltage Reference
W/L - Word Limit
Write Inh. - Write Inhibit

Table B-3. Cross-Reference Chart of Number Bases

Binary	Octal	Hexadecimal	Decimal	Standard Abbreviation
0000	0	0	0	
0001	1	1	1	
0010	2	2	2	
0011	3	3	3	
0100	4	4	4	
0101	5	5	5	
0110	6	6	6	
0111	7	7	7	
1000	10	8	8	
1001	11	9	9	
1010	12	A	10	
1011	13	B	11	
1100	14	C	12	
1101	15	D	13	
1110	16	E	14	
1111	17	F	15	
0001 0000	20	10	16	
0010 0000	40	20	32	
0100 0000	100	40	64	
1000 0000	200	80	128	
0001 0000 0000	400	100	256	
0010 0000 0000	1000	200	512	
0100 0000 0000	2000	400	1,024	1K
1000 0000 0000	4000	800	2,048	2K
1100 0000 0000	6000	C00	3,072	3K
0001 0000 0000 0000	10000	1000	4,096	4K
0001 0100 0000 0000	12000	1400	5,120	5K
0001 1000 0000 0000	14000	1800	6,144	6K
0001 1100 0000 0000	16000	1C00	7,168	7K
0010 0000 0000 0000	20000	2000	8,192	8K
0010 0100 0000 0000	22000	2400	9,216	9K
0010 1000 0000 0000	24000	2800	10,240	10K
0100 0000 0000 0000	40000	4000	16,384	16K
1000 0000 0000 0000	100000	8000	32,768	32K
0001 0000 0000 0000 0000	200000	10000	65,536	64K

Table B-4. ASCII & IEEE CODE CHART



7 6 5 / BITS 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS & SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 ` 60 96	160 p 70 112
0 0 0 1	1 SOH 1 1	21 DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
0 0 1 0	2 STX 2 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
0 0 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
0 1 0 0	4 EOT 4 4	24 DC4 14 20	44 $ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
0 1 0 1	5 ENQ 5 5	25 NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
0 1 1 0	6 ACK 6 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
0 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 0 0 0	10 BS 8 8	30 CAN 18 24	50 (28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
1 0 0 1	11 HT 9 9	31 EM 19 25	51) 29 41	71 9 39 57	111 I 49 73	131 Y 59 89	151 i 69 105	171 y 79 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [5B 91	153 k 6B 107	173 { 7B 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 V 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174 | 7C 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 - 2D 45	75 = 3D 61	115 M 4D 77	135] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	77 ? 3F 63	117 O 4F 79	137 _ 5F 95	157 o 6F 111	177 Rubout 7F 127
	Addressed Commands	Universal Commands	Listen Addresses		Talk Addresses		Secondary Addresses or Commands	

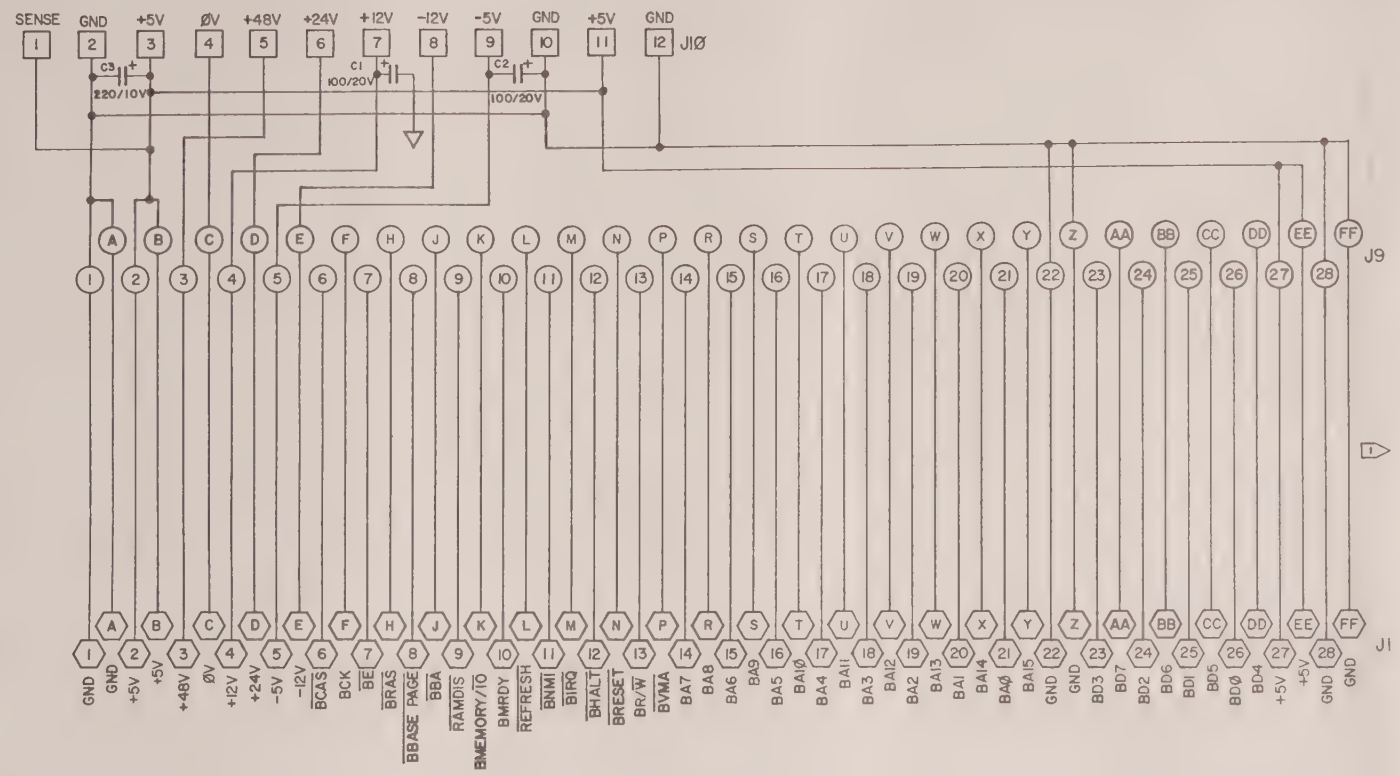
Table B-5. ASCII CONTROL CHARACTERS

ACK	acknowledge
BEL	bell
BS	backspace
CAN	cancel
CR	carriage return
DC1	playback on, CNTL Q, X-ON
DC2	record on, CNTL R, PUNCH-ON, SOM
DC3	playback off, CNTL S, X-OFF
DC4	record off, CNTL T, PUNCH-OFF, EOM
DEL	delete, rubout
DLE	data link escape
EM	end of medium
ENQ	enquiry
EOT	end of transmission
ESC	escape
ETB	end of transmission block
ETX	end of text
FF	form feed
FS	file separater
GS	group separater
HT	horizontal tabulation
LF	line feed
NAK	negative acknowledge
NUL	null
RS	record separater
SI	shift in
SO	shift out
SOH	start of heading
STX	start of text
SUB	substitute
SYN	synchronous idle
US	unit separater
VT	vertical tab

APPENDIX C
SCHEMATICS
PROGRAMMER BOARDS

30-702-0192	Mother Board
30-701-1647	6809E CPU
30-701-1826	EPROM
30-701-1827	16/32K Dynamic RAM
30-701-1829	Keyboard Display/Display Interface and Asynchronous Serial Port
30-701-1830	Dual Serial I/O (121A Only)
30-702-1835	Specific I/O
30-702-1643	Regulator 201
30-702-1644	Regulator 301
30-702-1645	Power Supply Bridge
30-702-1642	Keyboard
30-702-1649	FIP Display Driver
30-702-0060	Display
30-702-1640	Digital/Analog Driver (Programming Electronics)
30-702-1641	Socket Board
30-701-1631	RAM Disk
30-701-1673	D/A Driver

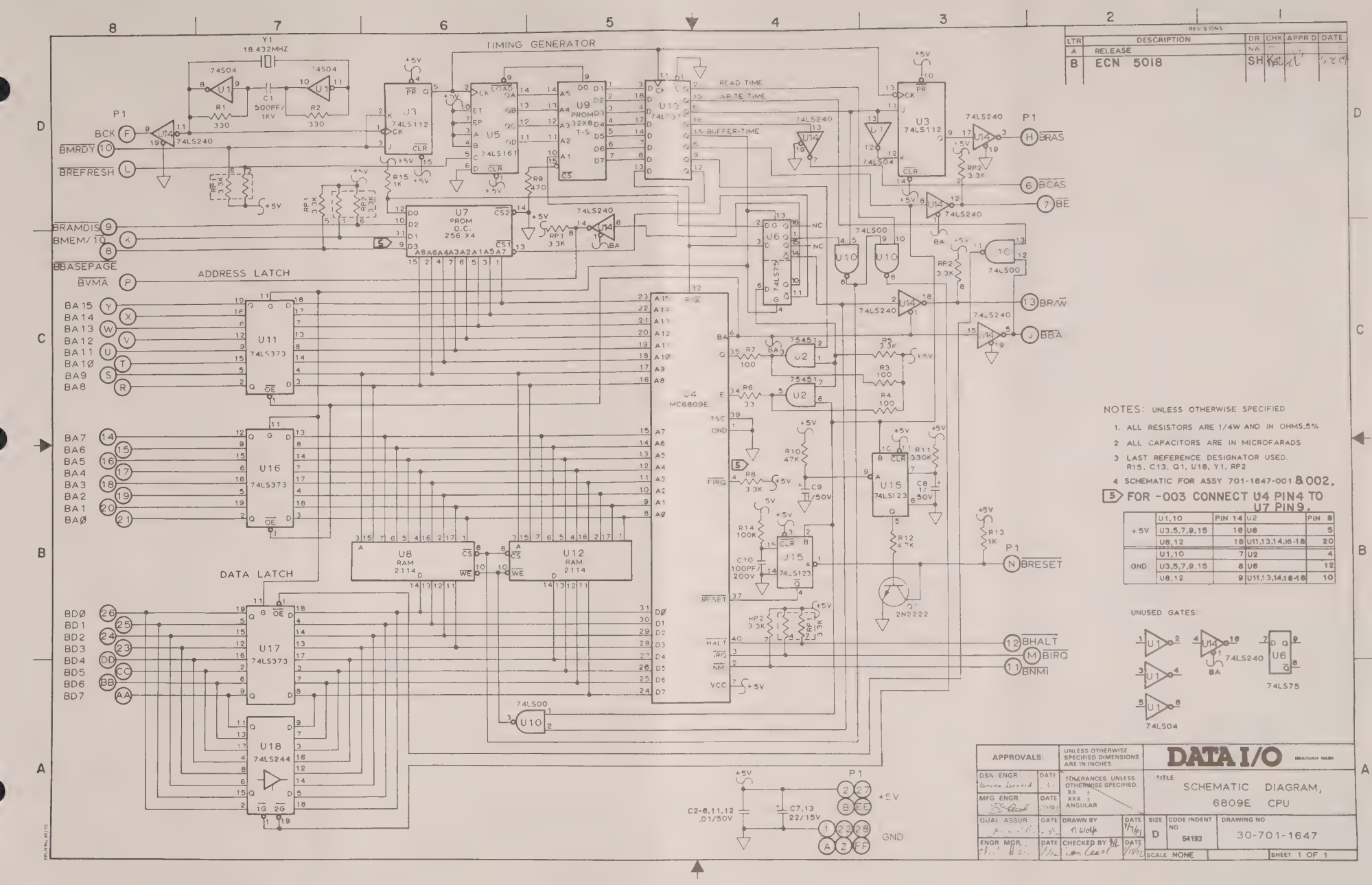
REVISIONS				
ZONE	LTR	DESCRIPTION	CM.	PE	DATE
	A	RELEASE			10-80


SENSE GND +5V ØV +48V +24V +12V -12V -5V GND +5V GND J1Ø
1 2 3 4 5 6 7 8 9 10 11 12
C3 220/10V
C1 100/20V
C2 100/20V
A B C D E F H J K L M N P R S T U V W X Y Z AA BB CC DD EE FF J9
1
A B C D E F H J K L M N P R S T U V W X Y Z AA BB CC DD EE FF J1
GND GND +5V +5V +48V ØV +12V +24V -5V -12V BCAS BCK BE BRAS BBASE PAGE BBA RAMDIS BMEMORY/IO BMRDY REFRESH BNMI BIRQ BHALT BRESET BR/W BVMA BA7 BA8 BA6 BA9 BA5 BAIØ BA4 BAII BA3 BAI2 BA2 BA13 BAI BAI4 BAØ BAI5 GND GND BD3 BD7 BD2 BD6 BDI BD5 BDØ BD4 +5V +5V GND GND

NOTES:

1. J2 THRU J8 OMITTED FOR CLARITY
2. -001 OMIT J1-3.
3. -002 SHOWN
4. ALL CAPACITORS ARE IN MICROFARADS.

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ ENG.	TOLERANCES DECIMALS ANGULAR X ± XX ± XXX ± DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM MOTHER BOARD	
ENG. MGR.		SIZE D	CODE IDENT NO 54193	DRAWING NO 30-702-0192
Q C	DRAWN BY Barry Tibbitts	SCALE —	SHEET 1 OF 1
DATE 10-10-80	CHECKED BY		



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	NW			
B	ECN 5018	SH			

NOTES: UNLESS OTHERWISE SPECIFIED

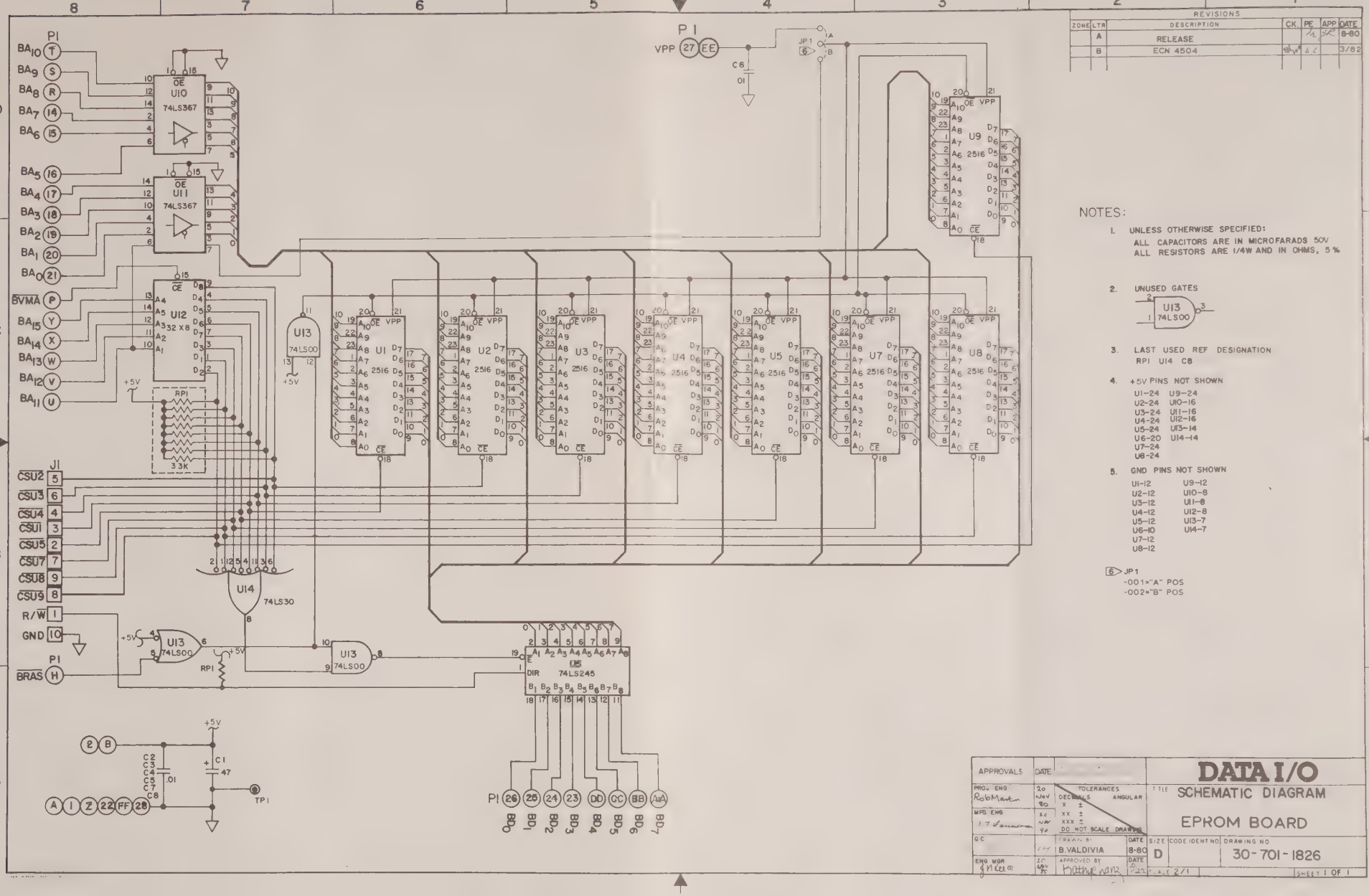
1. ALL RESISTORS ARE 1/4W AND IN OHMS,5%
2. ALL CAPACITORS ARE IN MICROFARADS
3. LAST REFERENCE DESIGNATOR USED. R15, C13, Q1, U18, Y1, RP2
4. SCHEMATIC FOR ASSY 701-1647-001 & 002.
5. FOR -003 CONNECT U4 PIN4 TO U7 PIN9.

+5V	U1,10	PIN 14	U2	PIN 8
	U3,5,7,9,15	16	U8	5
	U8,12	18	U11,13,14,16-18	20
GND	U1,10	7	U2	4
	U3,5,7,9,15	8	U8	12
	U8,12	9	U11,13,14,16-18	10

UNUSED GATES:

74LS04 74LS240 74LS75

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O REDMOND WASH
DSN ENGR	TOLERANCES UNLESS OTHERWISE SPECIFIED. XX ± XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, 6809E CPU
MFG ENGR		
QUAL ASSUR	DRAWN BY	SIZE D; CODE IDENT NO 54193; DRAWING NO 30-701-1647
ENGR MGR	CHECKED BY	SCALE NONE; SHEET 1 OF 1



REVISIONS					
ZONE	LTR	DESCRIPTION	CK.	PE	APP'D DATE
	A	RELEASE			8-80
	B	ECN 4504			3/82

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITORS ARE IN MICROFARADS 50V
   ALL RESISTORS ARE 1/4W AND IN OHMS, 5%
2. UNUSED GATES
   U13 74LS00
3. LAST USED REF DESIGNATION
   RP1 U14 C8
4. +5V PINS NOT SHOWN

U1-24	U9-24
U2-24	U10-16
U3-24	U11-16
U4-24	U12-16
U5-24	U13-14
U6-20	U14-14
U7-24	
U8-24	

5. GND PINS NOT SHOWN

U1-12	U9-12
U2-12	U10-8
U3-12	U11-8
U4-12	U12-8
U5-12	U13-7
U6-10	U14-7
U7-12	
U8-12	

6 JP1
-001="A" POS
-002="B" POS

APPROVALS	DATE
PROJ. ENG. Rob Martin	
MFG. ENG. I.T. Lawrence	
Q.C.	
ENG. MGR. S. McGee	

TOLERANCES: DECIMALS X ±, XX ±, XXX ±; ANGULAR ±; DO NOT SCALE DRAWING

DRAWN BY: B. VALDIVIA — DATE 8-80

APPROVED BY: Matthew Ward — DATE 8/22

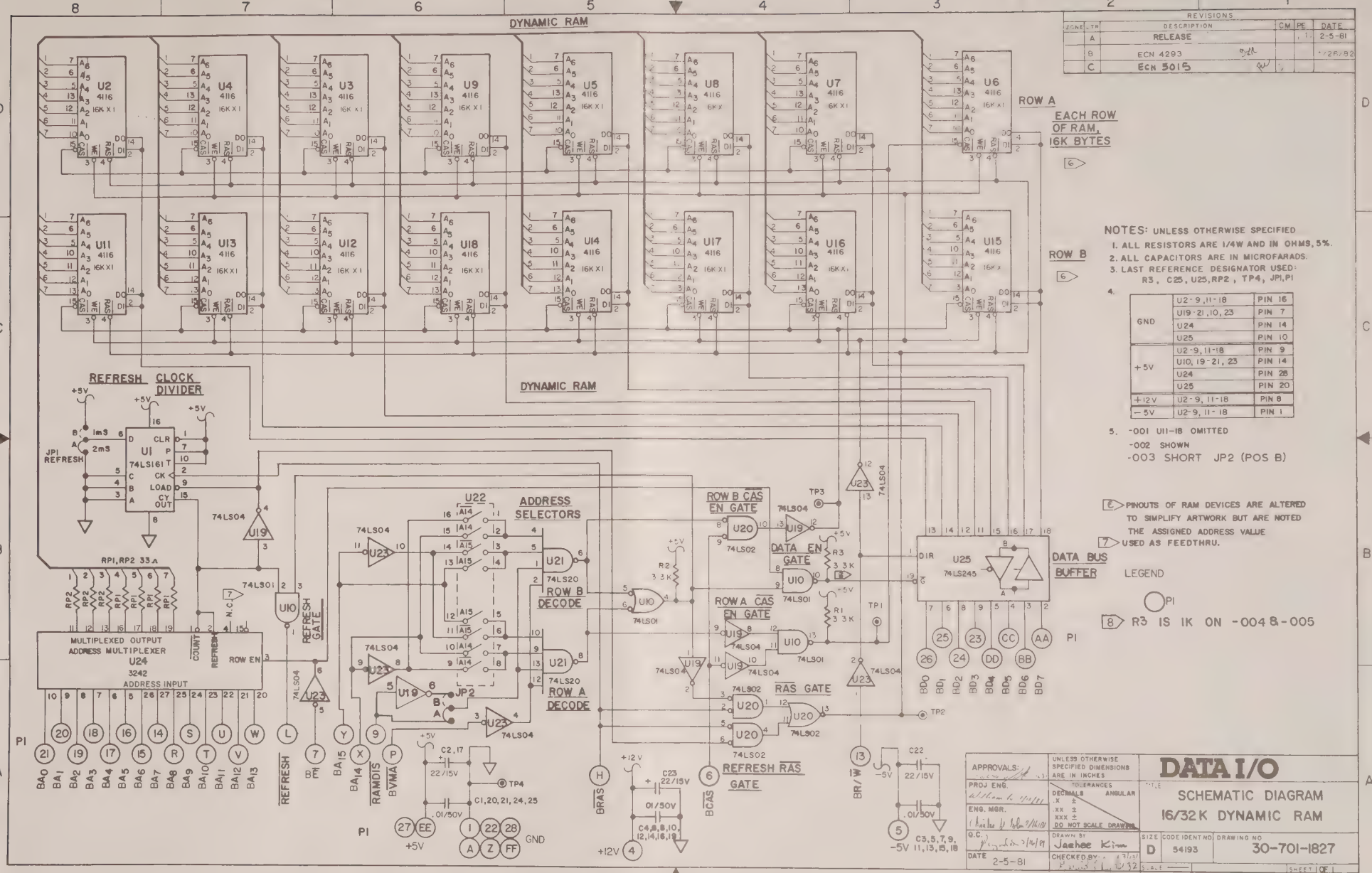
DATA I/O

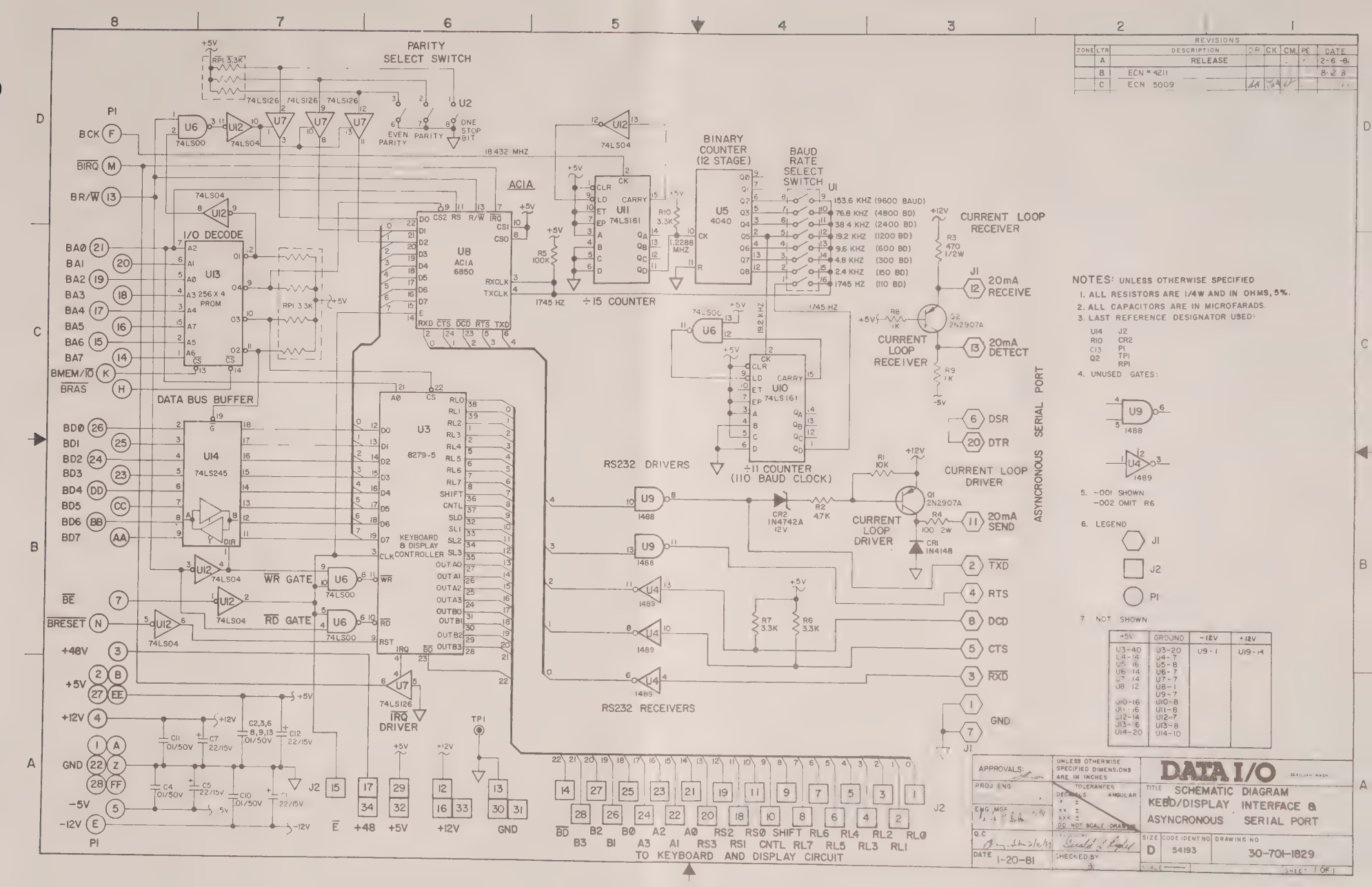
TITLE: SCHEMATIC DIAGRAM

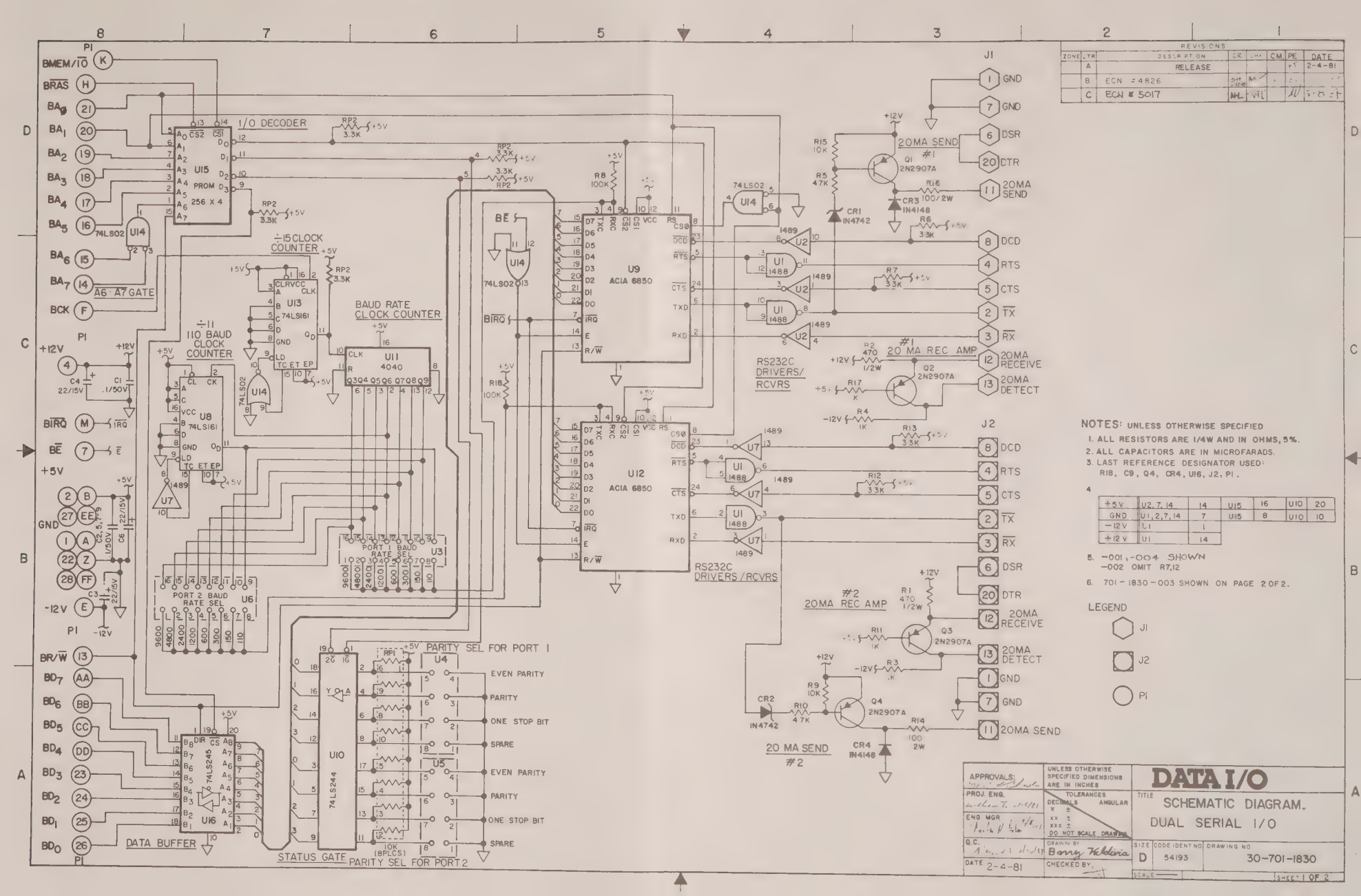
EPROM BOARD

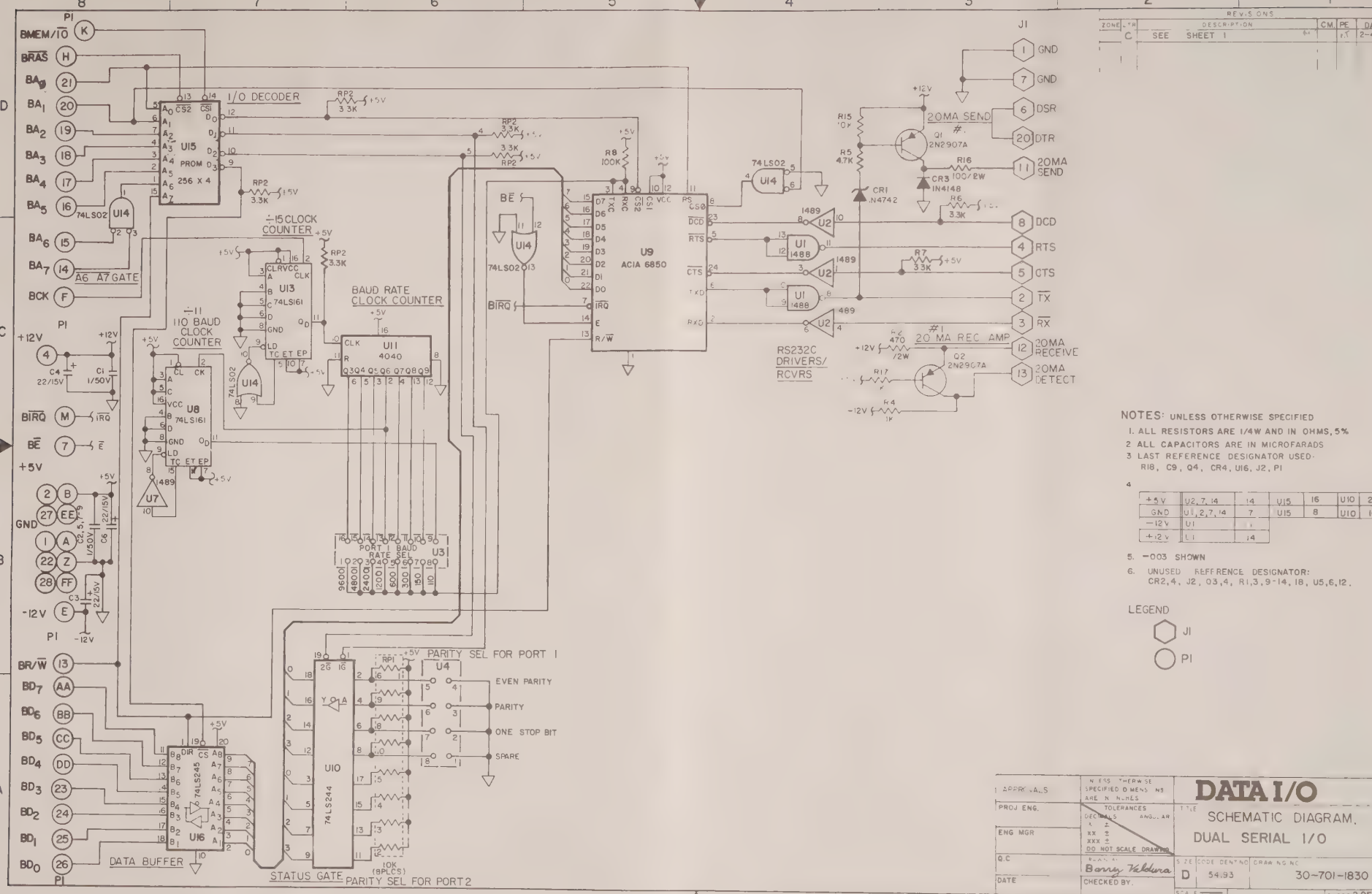
SIZE D | CODE IDENT NO. | DRAWING NO. 30-701-1826

SCALE 2/1 | SHEET 1 OF 1


DYNAMIC RAM
REVISIONS
ZONE LTR | DESCRIPTION | CM | PE | DATE
A | RELEASE | | | 2-5-81
B | ECN 4293 | | | 1/26/82
C | ECN 5015 | | |
ROW A
EACH ROW OF RAM, 16K BYTES
ROW B
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: R3, C25, U25, RP2, TP4, JP1, P1
4.
GND | U2-9, 11-18 | PIN 16
U19-21, 10, 23 | PIN 7
U24 | PIN 14
U25 | PIN 10
+5V | U2-9, 11-18 | PIN 9
U10, 19-21, 23 | PIN 14
U24 | PIN 28
U25 | PIN 20
+12V | U2-9, 11-18 | PIN 8
-5V | U2-9, 11-18 | PIN 1
5. -001 U11-18 OMITTED
-002 SHOWN
-003 SHORT JP2 (POS B)
PINOUTS OF RAM DEVICES ARE ALTERED TO SIMPLIFY ARTWORK BUT ARE NOTED THE ASSIGNED ADDRESS VALUE
USED AS FEEDTHRU.
LEGEND
P1
R3 IS 1K ON -004 & -005
REFRESH CLOCK DIVIDER
JP1 REFRESH
74LS161
74LS04
74LS01
74LS20
74LS02
74LS245
DATA BUS BUFFER
ADDRESS SELECTORS
ROW B DECODE
ROW A DECODE
ROW B CAS EN GATE
ROW A CAS EN GATE
DATA EN GATE
RAS GATE
REFRESH RAS GATE
REFRESH GATE
MULTIPLEXED OUTPUT ADDRESS MULTIPLEXER U24 3242
ADDRESS INPUT
RP1, RP2 33Δ
BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7 BA8 BA9 BA10 BA11 BA12 BA13
REFRESH
RAMDIS
BVMA
BRAS
BCAS
BR/W
BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7
APPROVALS:
PROJ ENG.
ENG. MGR.
Q.C.
DATE 2-5-81
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS ANGULAR
.X ±
.XX ±
.XXX ±
DO NOT SCALE DRAWING
DRAWN BY Jaehee Kim
CHECKED BY
DATA I/O
TITLE
SCHEMATIC DIAGRAM
16/32K DYNAMIC RAM
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1827
SCALE
SHEET 1 OF 1


PARITY SELECT SWITCH
ACIA
I/O DECODE
DATA BUS BUFFER
BINARY COUNTER (12 STAGE)
BAUD RATE SELECT SWITCH
÷15 COUNTER
÷11 COUNTER (110 BAUD CLOCK)
KEYBOARD & DISPLAY CONTROLLER
IRQ DRIVER
WR GATE
RD GATE
RS232 DRIVERS
RS232 RECEIVERS
CURRENT LOOP RECEIVER
CURRENT LOOP DRIVER
ASYNCRONOUS SERIAL PORT
TO KEYBOARD AND DISPLAY CIRCUIT
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
4. UNUSED GATES:
5. -001 SHOWN -002 OMIT R6
6. LEGEND
7. NOT SHOWN
REVISIONS
DATA I/O
SCHEMATIC DIAGRAM KEBD/DISPLAY INTERFACE & ASYNCRONOUS SERIAL PORT
DRAWING NO 30-701-1829
DATE 1-20-81


REVISIONS
ZONE | LTR | DESCRIPTION | DR | CHK | CM | PE | DATE
A | RELEASE | | | | PT | 2-4-81
B | ECN # 4826 | SHT 1 DEMO | BK | | | | 5-8-81
C | ECN # 5017 | MHL | VHL | | MM | 5-8-81
I/O DECODER
÷15 CLOCK COUNTER
÷11 110 BAUD CLOCK COUNTER
BAUD RATE CLOCK COUNTER
A6 · A7 GATE
PORT 1 BAUD RATE SEL
PORT 2 BAUD RATE SEL
DATA BUFFER
STATUS GATE
PARITY SEL FOR PORT 1
PARITY SEL FOR PORT 2
RS232C DRIVERS/RCVRS
RS232C DRIVERS/ RCVRS
#1 20 MA REC AMP
#2 20MA REC AMP
20MA SEND #1
20 MA SEND #2
J1
J2
P1
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: R18, C9, Q4, CR4, U16, J2, P1.
4
+5V | U2,7,14 | 14 | U15 | 16 | U10 | 20
GND | U1,2,7,14 | 7 | U15 | 8 | U10 | 10
-12V | U1 | 1
+12V | U1 | 14
5. -001,-004 SHOWN -002 OMIT R7,12
6. 701-1830-003 SHOWN ON PAGE 2 OF 2.
LEGEND
J1
J2
P1
APPROVALS:
PROJ. ENG.
ENG MGR
Q.C.
DATE 2-4-81
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS X ± XX ± XXX ±
ANGULAR ±
DO NOT SCALE DRAWING
DRAWN BY Barry Kelderia
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM, DUAL SERIAL I/O
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1830
SCALE
SHEET 1 OF 2



REVISIONS				
ZONE	LTR	DESCRIPTION	CM	PE	DATE
C		SEE SHEET 1			2-4-81

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%
2. ALL CAPACITORS ARE IN MICROFARADS
3. LAST REFERENCE DESIGNATOR USED: R18, C9, Q4, CR4, U16, J2, P1
4.

+5V	U2, 7, 14	14	U15	16	U10	20
GND	U1, 2, 7, 14	7	U15	8	U10	10
-12V	U1	1				
+12V	L1	14				

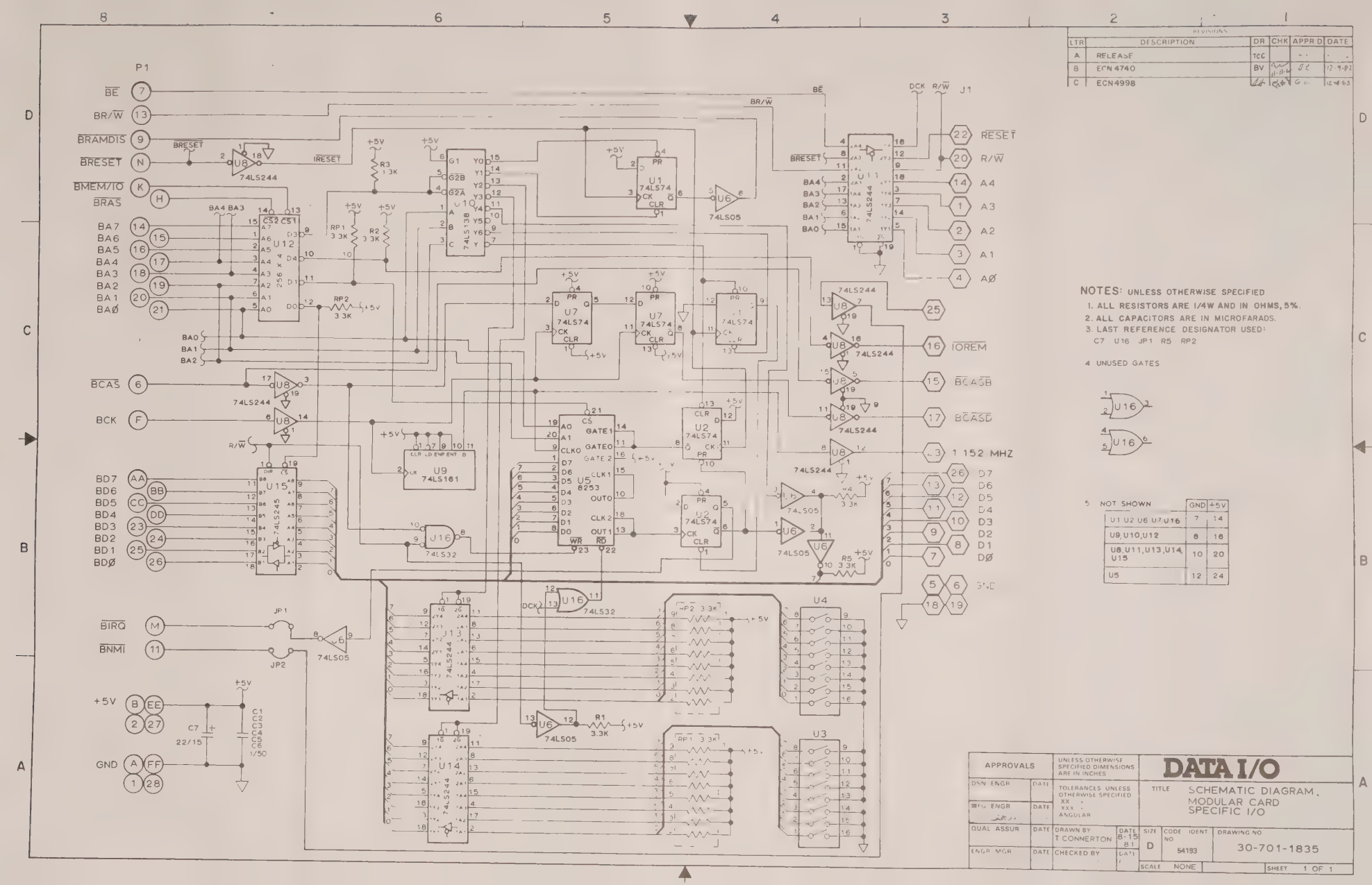
5. -003 SHOWN
6. UNUSED REFFERENCE DESIGNATOR: CR2,4, J2, Q3,4, R1,3,9-14, 18, U5,6,12.

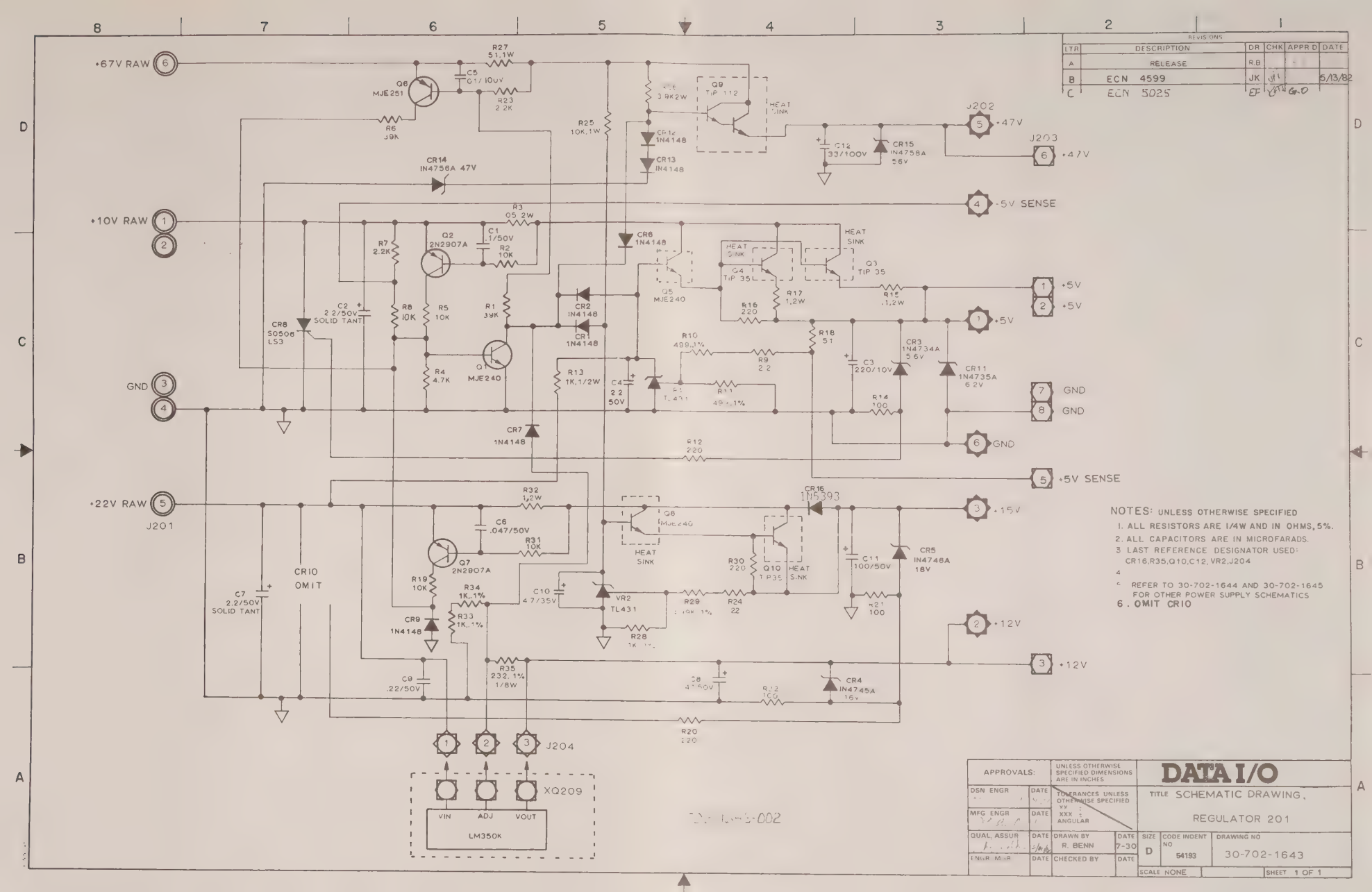
LEGEND

JI

PI

APPROVALS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ ENG.	TOLERANCES DECIMALS ANGULAR .X ± .XX ± .XXX ± DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM, DUAL SERIAL I/O	
ENG MGR	DRAWN Barry Veldura	SIZE D	CODE IDENT NO 54193
Q.C	CHECKED BY	DRAWING NO 30-701-1830	
DATE	SCALE	SHEET 2 OF 2	


P1
BE
BR/W
BRAMDIS
BRESET
BMEM/IO
BRAS
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BAØ
BCAS
BCK
R/W
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BDØ
BIRQ
BNMI
+5V
GND
JP1
JP2
74LS244
74LS245
74LS138
74LS574
74LS161
74LS32
74LS05
8253
256 X 4
RP1 3 3K
RP2 3 3K
R1 3.3K
R2 3 3K
R3 1 3K
R5 3 3K
C7 22/15
C1 C2 C3 C4 C5 C6 1/50
J1
RESET
R/W
A4
A3
A2
A1
AØ
IOREM
BCASB
BCASD
1 152 MHZ
D7
D6
D5
D4
D3
D2
D1
DØ
GND
U1 U2 U6 U7 U16
U9,U10,U12
U8,U11,U13,U14,U15
U5
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
C7 U16 JP1 R5 RP2
4 UNUSED GATES
5 NOT SHOWN
REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
A RELEASE TCC 12-9-82
B ECN 4740 BV 12-14-83
C ECN 4998
APPROVALS
DSN ENGR
SFTG ENGR
QUAL ASSUR
ENGR MGR
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
DRAWN BY T CONNERTON
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM, MODULAR CARD SPECIFIC I/O
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1835
SCALE NONE
SHEET 1 OF 1



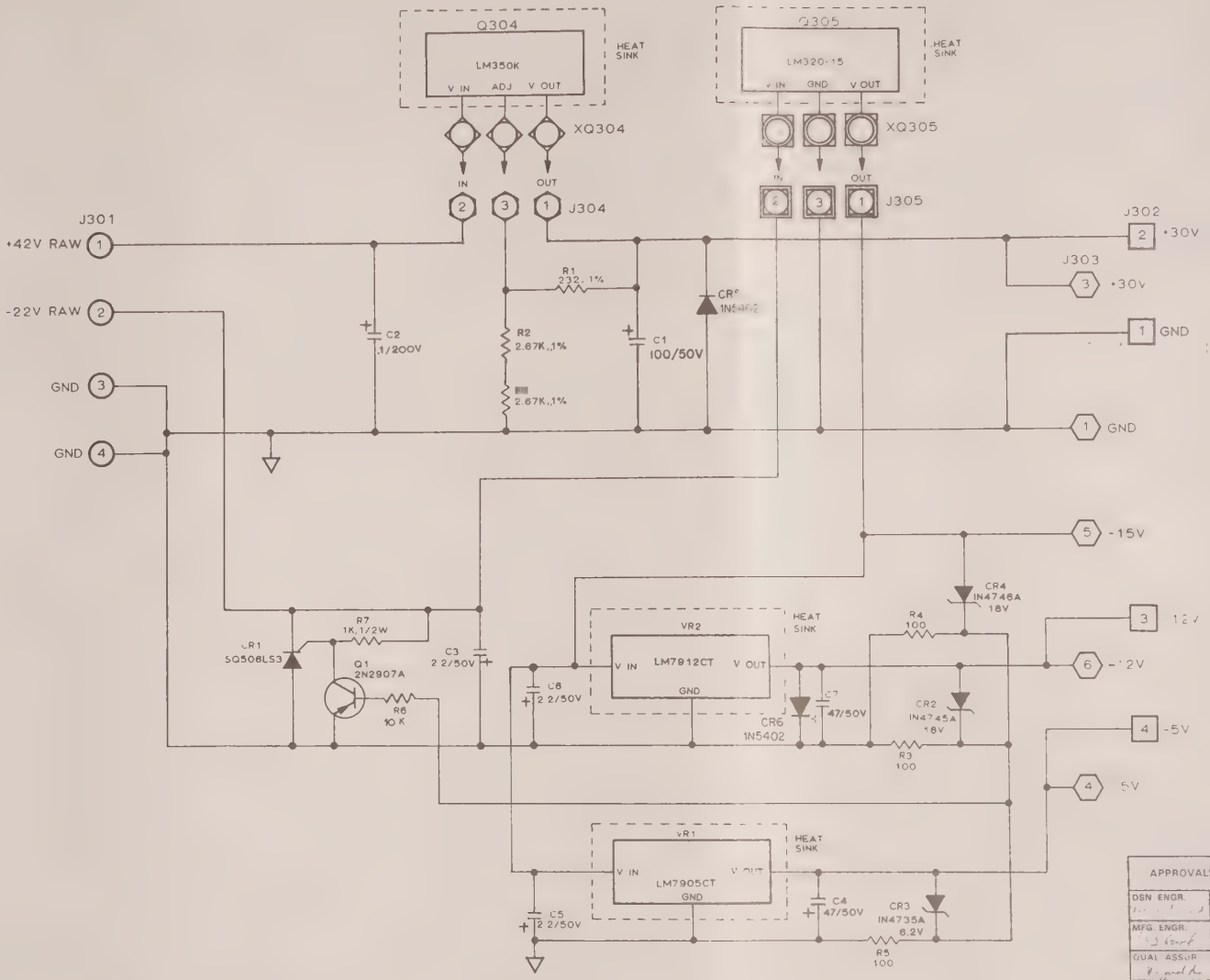
REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	R.B			
B	ECN 4599	JK			5/13/82
C	ECN 5025	EF			

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: CR16, R35, Q10, C12, VR2, J204
4.
5. REFER TO 30-702-1644 AND 30-702-1645 FOR OTHER POWER SUPPLY SCHEMATICS
6. OMIT CR10

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR / DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED .xx ± .xxx ± ANGULAR	TITLE SCHEMATIC DRAWING, REGULATOR 201	
MFG ENGR / DATE			
QUAL. ASSUR / DATE	DRAWN BY R. BENN / DATE 7-30	SIZE D	CODE INDENT NO 54193
ENGR. MGR / DATE	CHECKED BY / DATE	DRAWING NO 30-702-1643	
		SCALE NONE	SHEET 1 OF 1

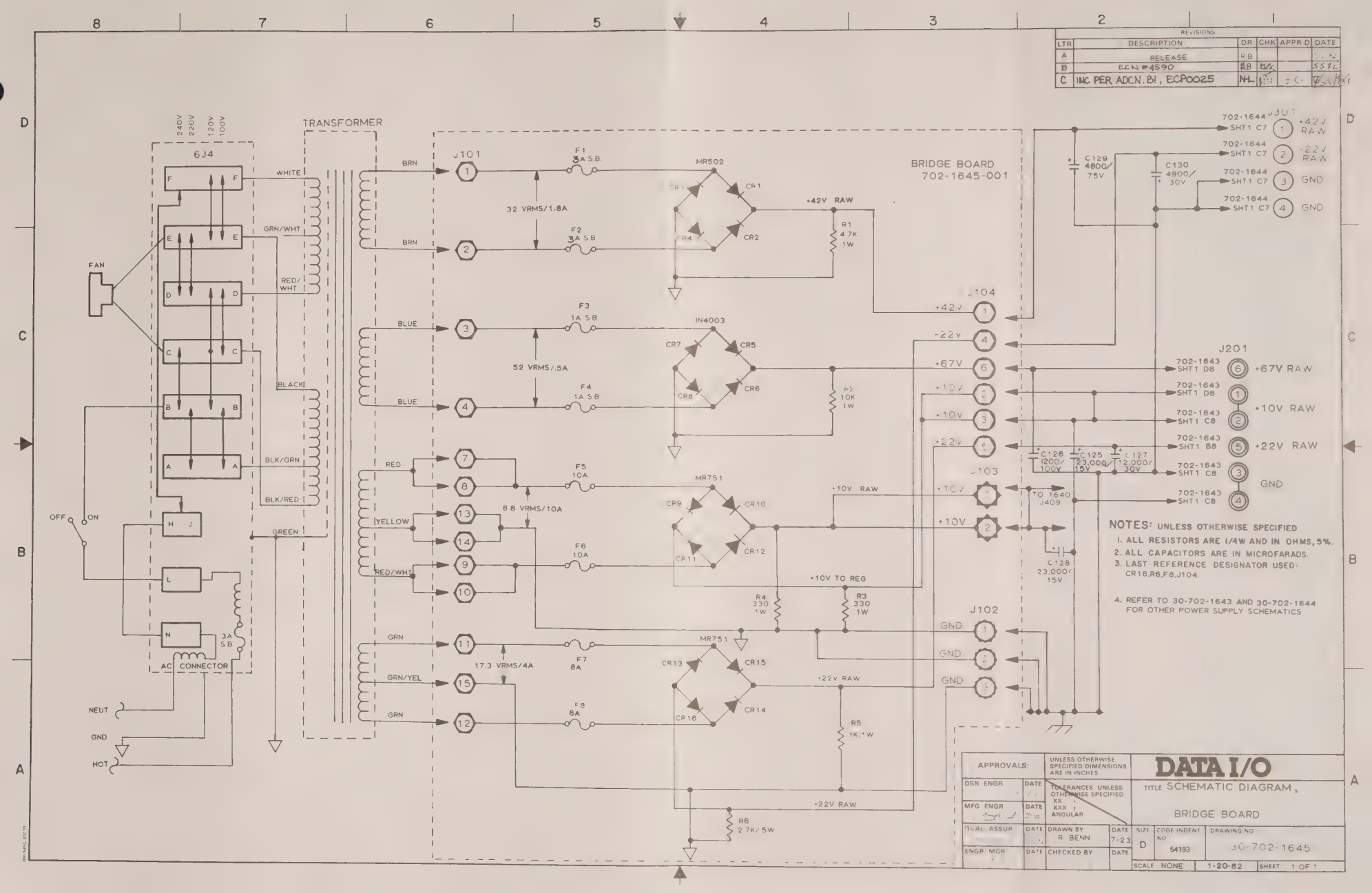
REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	RB	TE	AT	
B	ECN 4701 9-2-82	SM			
C	ECN4740	BV			
D	ECN 4836 CMA 0026	CL			

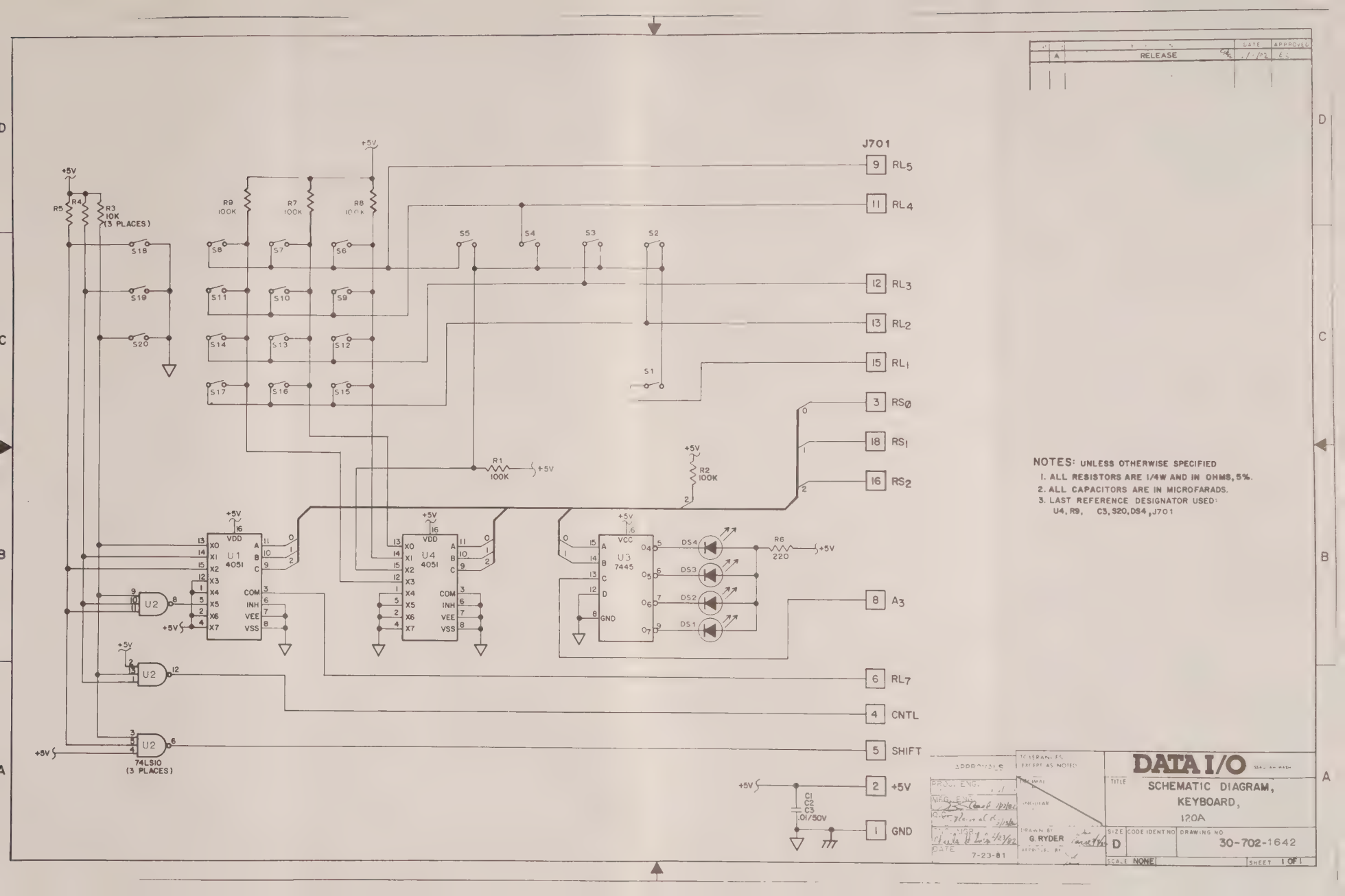


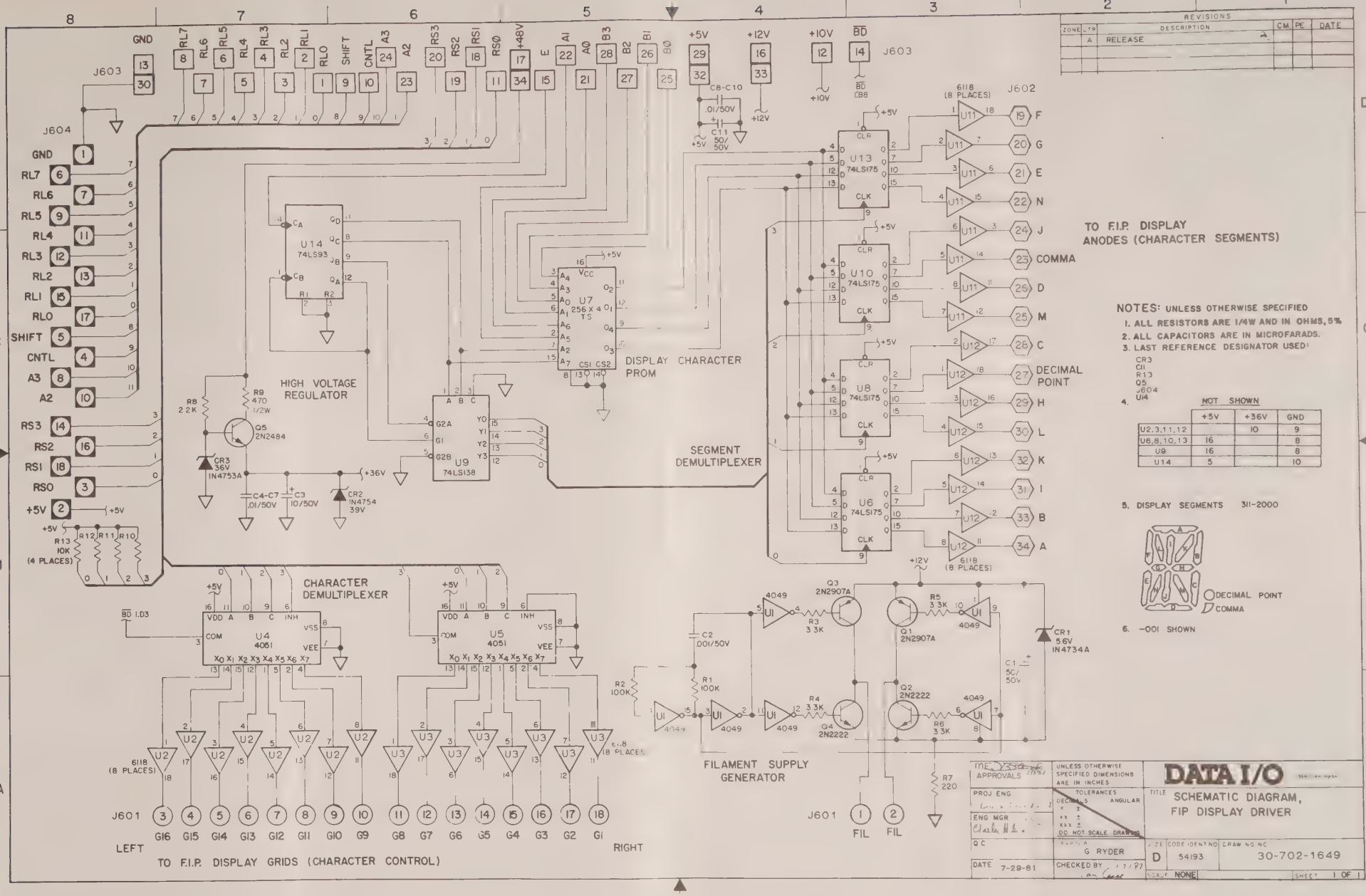
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: CR6 ,R8,Q1,C7,VR2 , J305
4. 702-1644-003 SHOWN.
5. REFER TO 30-702-1643 AND 30-702-1645 FOR OTHER POWER SUPPLY SCHEMATICS.

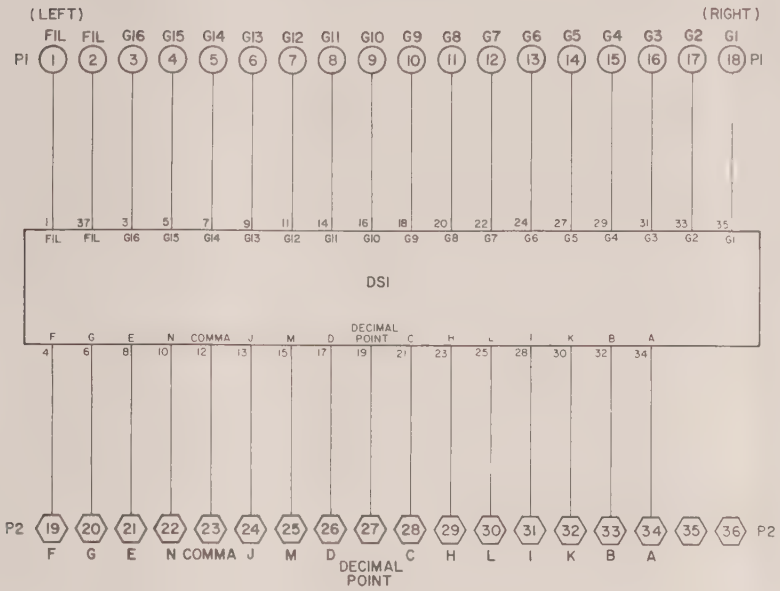
APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O			
DSN ENGR.	DATE 1/21/82	TOLERANCES UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR		TITLE SCHEMATIC DIAGRAM, REGULATOR 301			
MFG. ENGR.	DATE 1/21/82						
QUAL ASSUR	DATE 1/21/82	DRAWN BY R. BENN	DATE 7-24	SIZE D	CODE IDENT NO. 54193	DRAWING NO 30-702-1644	
ENGR MGR.	DATE 1/21/82	CHECKED BY:	DATE 7/1/82	SCALE NONE	1-21-82	SHEET 1 OF 1	


REVISIONS
LTR DESCRIPTION DR CHK APPR D DATE
A RELEASE RB
B E.C.N #4590 RB
C INC PER ADCN. B1, ECP0025 NL
240V 220V 120V 100V
TRANSFORMER
6J4
WHITE
GRN/WHT
RED/WHT
BLACK
BLK/GRN
BLK/RED
GREEN
FAN
OFF ON
AC CONNECTOR
3A SB
NEUT
GND
HOT
J101
BRN
BRN
BLUE
BLUE
RED
YELLOW
RED/WHT
GRN
GRN/YEL
GRN
32 VRMS/1.8A
52 VRMS/.5A
8.8 VRMS/10A
17.3 VRMS/4A
F1 3A S.B.
F2 3A SB
F3 1A SB
F4 1A SB
F5 10A
F6 10A
F7 8A
F8 8A
BRIDGE BOARD
702-1645-001
MR502
IN4003
MR751
MR751
CR1
CR2
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
+42V RAW
R1 4.7K 1W
R2 10K 1W
+10V RAW
+10V TO REG
R4 330 1W
R3 330 1W
+22V RAW
R5 1K,1W
-22V RAW
R6 2.7K/5W
J104
+42V
-22V
+67V
+10V
+10V
+22V
J103
+10V
+10V
J102
GND
GND
GND
C129 4800/ 75V
C130 4900/ 30V
C126 1200/ 100V
C125 23,000/ 15V
C127 2,000/ 30V
C128 23,000/ 15V
TO 1640 J409
J201
702-1644 SHT1 C7 J30 1 +42V RAW
702-1644 SHT1 C7 2 -22V RAW
702-1644 SHT1 C7 3 GND
702-1644 SHT1 C7 4 GND
702-1643 SHT1 D8 6 +67V RAW
702-1643 SHT1 D8 1
702-1643 SHT1 C8 2 +10V RAW
702-1643 SHT1 B8 5 +22V RAW
702-1643 SHT1 C8 3
702-1643 SHT1 C8 4 GND
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: CR16,R6,F8,J104.
4. REFER TO 30-702-1643 AND 30-702-1644 FOR OTHER POWER SUPPLY SCHEMATICS
APPROVALS:
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR
DSN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
DRAWN BY R BENN 7-23
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM, BRIDGE BOARD
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-702-1645
SCALE NONE
1-20-82
SHEET 1 OF 1


J701
9 RL5
11 RL4
12 RL3
13 RL2
15 RL1
3 RSØ
18 RS1
16 RS2
8 A3
6 RL7
4 CNTL
5 SHIFT
2 +5V
1 GND
R1 100K
R2 100K
R3 10K (3 PLACES)
R4
R5
R6 220
R7 100K
R8 100K
R9 100K
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
U1 4051
U2
74LS10 (3 PLACES)
U3 7445
U4 4051
DS1
DS2
DS3
DS4
C1
C2
C3
.01/50V
+5V
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
U4, R9, C3, S20, DS4, J701
RELEASE
DATA I/O
SCHEMATIC DIAGRAM,
KEYBOARD,
120A
DRAWN BY G. RYDER
DATE 7-23-81
SIZE D
DRAWING NO 30-702-1642
SCALE NONE
SHEET 1 OF 1


REVISIONS
ZONE | LTR | DESCRIPTION | CM. | PE | DATE
A RELEASE
J603
J604
J602
J601
GND
RL7
RL6
RL5
RL4
RL3
RL2
RLI
RLO
SHIFT
CNTL
A3
A2
RS3
RS2
RSI
RSO
+5V
+48V
E
AI
A0
B3
B2
BI
B0
+12V
+10V
BD
BB
U14 74LS93
U7 256 X 4 TS
DISPLAY CHARACTER PROM
HIGH VOLTAGE REGULATOR
R8 2.2K
R9 470 1/2W
Q5 2N2484
CR3 36V IN4753A
CR2 IN4754 39V
C3 10/50V
C4-C7 .01/50V
C8-C10 .01/50V
C11 50/50V
U9 74LS138
SEGMENT DEMULTIPLEXER
U13 74LS175
U10 74LS175
U8 74LS175
U6 74LS175
6118 (8 PLACES)
TO F.I.P. DISPLAY ANODES (CHARACTER SEGMENTS)
F
G
E
N
J
COMMA
D
M
C
DECIMAL POINT
H
L
K
I
B
A
R13 10K (4 PLACES)
R12
R11
R10
CHARACTER DEMULTIPLEXER
U4 4051
U5 4051
6118 (8 PLACES)
U2
U3
J601
LEFT
RIGHT
G16 G15 G14 G13 G12 G11 G10 G9 G8 G7 G6 G5 G4 G3 G2 G1
TO F.I.P. DISPLAY GRIDS (CHARACTER CONTROL)
FILAMENT SUPPLY GENERATOR
Q1 2N2907A
Q2 2N2222
Q3 2N2907A
Q4 2N2222
R1 100K
R2 100K
R3 3.3K
R4 3.3K
R5 3.3K
R6 3.3K
R7 220
C1 5C/50V
C2 .001/50V
CR1 5.6V IN4734A
FIL
FIL
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: CR3 CII R13 Q5 J604 U14
4. NOT SHOWN
U2,3,11,12 | | 10 | 9
U6,8,10,13 | 16 | | 8
U9 | 16 | | 8
U14 | 5 | | 10
5. DISPLAY SEGMENTS 311-2000
DECIMAL POINT
COMMA
6. -001 SHOWN
APPROVALS
PROJ ENG
ENG MGR
QC
DATE 7-29-81
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS ANGULAR
DO NOT SCALE DRAWING
DRAWN G RYDER
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM, FIP DISPLAY DRIVER
SIZE D
CODE IDENT NO 54193
DRAW NO 30-702-1649
SCALE NONE
SHEET 1 OF 1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE				2-81



NOTES:

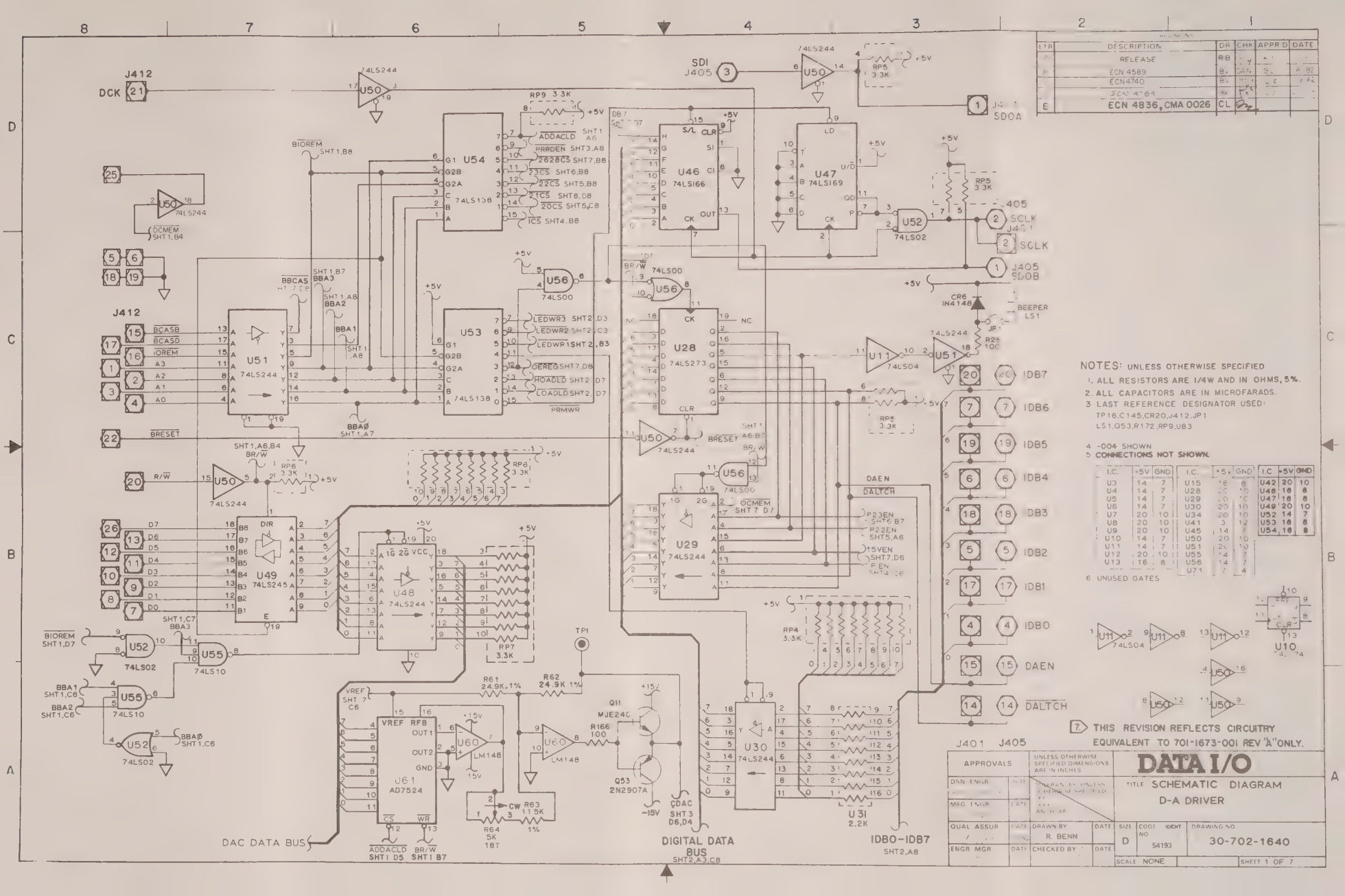
1. DISPLAY SEGMENTS 311-2000

2 -001 SHOWN

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O ISSAQUAH WASH
DSN. ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM FIP DISPLAY
MFG. ENGR	DATE		
QUALITY ASSUR	DATE	DRAWN BY B. Swindells	DATE 2-9-81
ENGR. MGR	DATE	CHECKED BY	DATE

SIZE	CODE IDENT NO	DRAWING NO
D	54193	30-702-0060

SCALE —— SHEET 1 OF 1



LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	RB			
B	ECN 4589	BL	CMA	SL	A 82
C	ECN 4740	BL			
D	ECN 4864	BL			
E	ECN 4836, CMA 0026	CL			

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
   TP16,C145,CR20,J412,JP1
   LS1,Q53,R172,RP9,U83
4. -004 SHOWN
5. CONNECTIONS NOT SHOWN.

I.C.	+5V	GND
U3	14	7
U4	14	7
U5	14	7
U6	14	7
U7	20	10
U8	20	10
U9	20	10
U10	14	7
U11	14	7
U12	20	10
U13	16	8

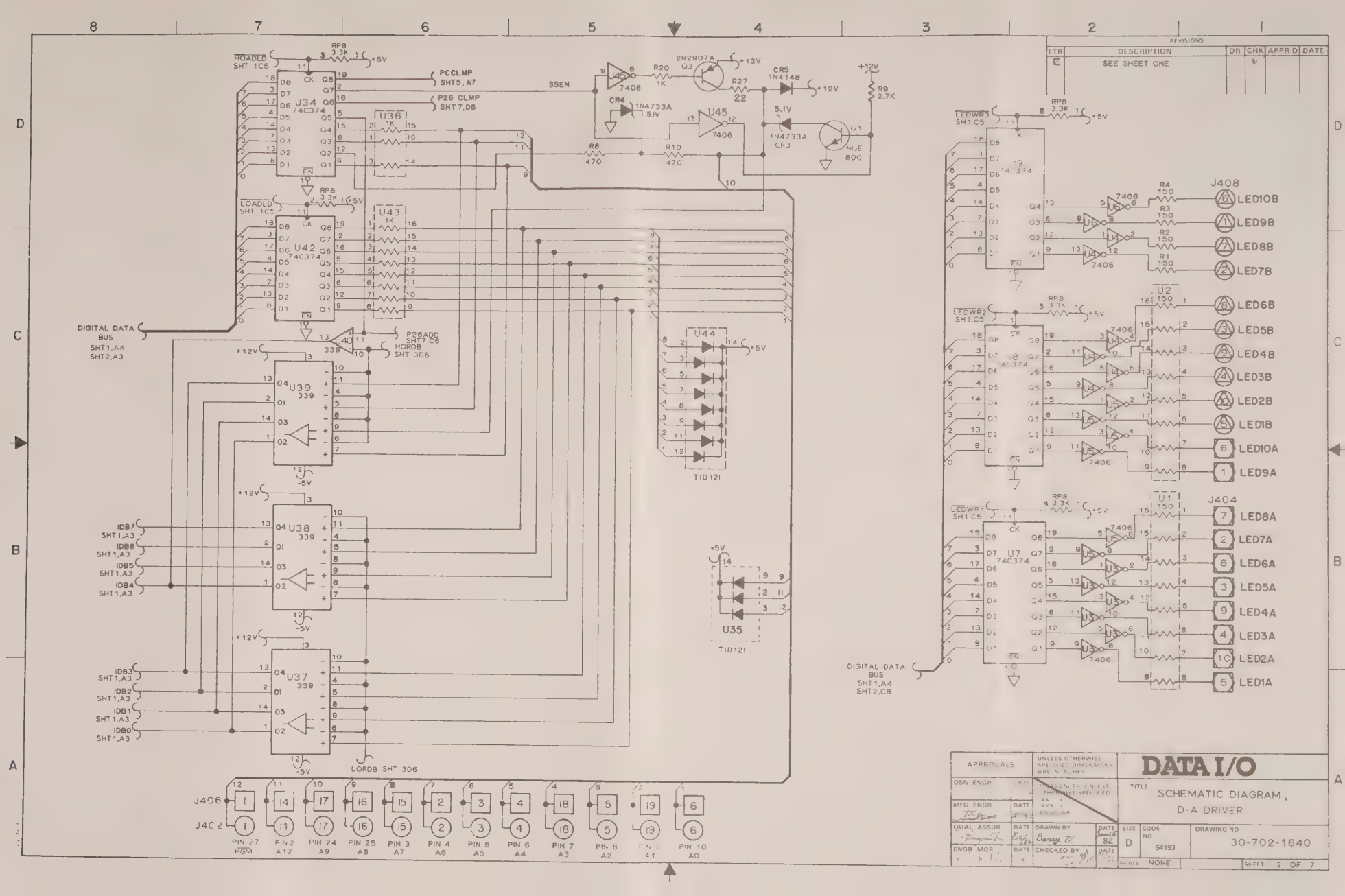
I.C.	+5V	GND
U15	16	8
U28	20	10
U29	20	10
U30	20	10
U34	20	10
U41	3	12
U45	14	7
U50	20	10
U51	20	10
U55	14	7
U56	14	7
U71	7	4

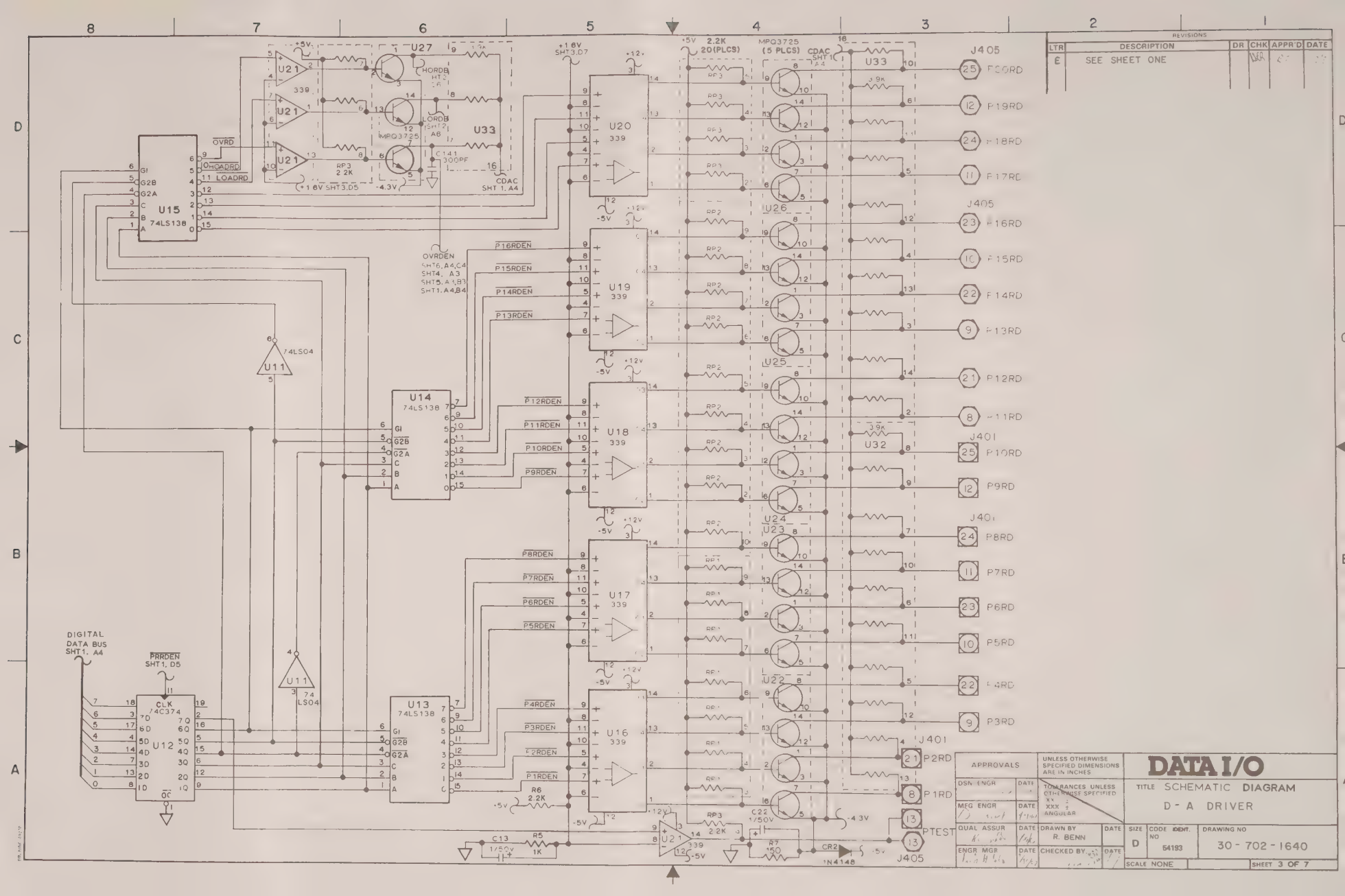
I.C.	+5V	GND
U42	20	10
U46	16	8
U47	16	8
U49	20	10
U52	14	7
U53	16	8
U54	16	8

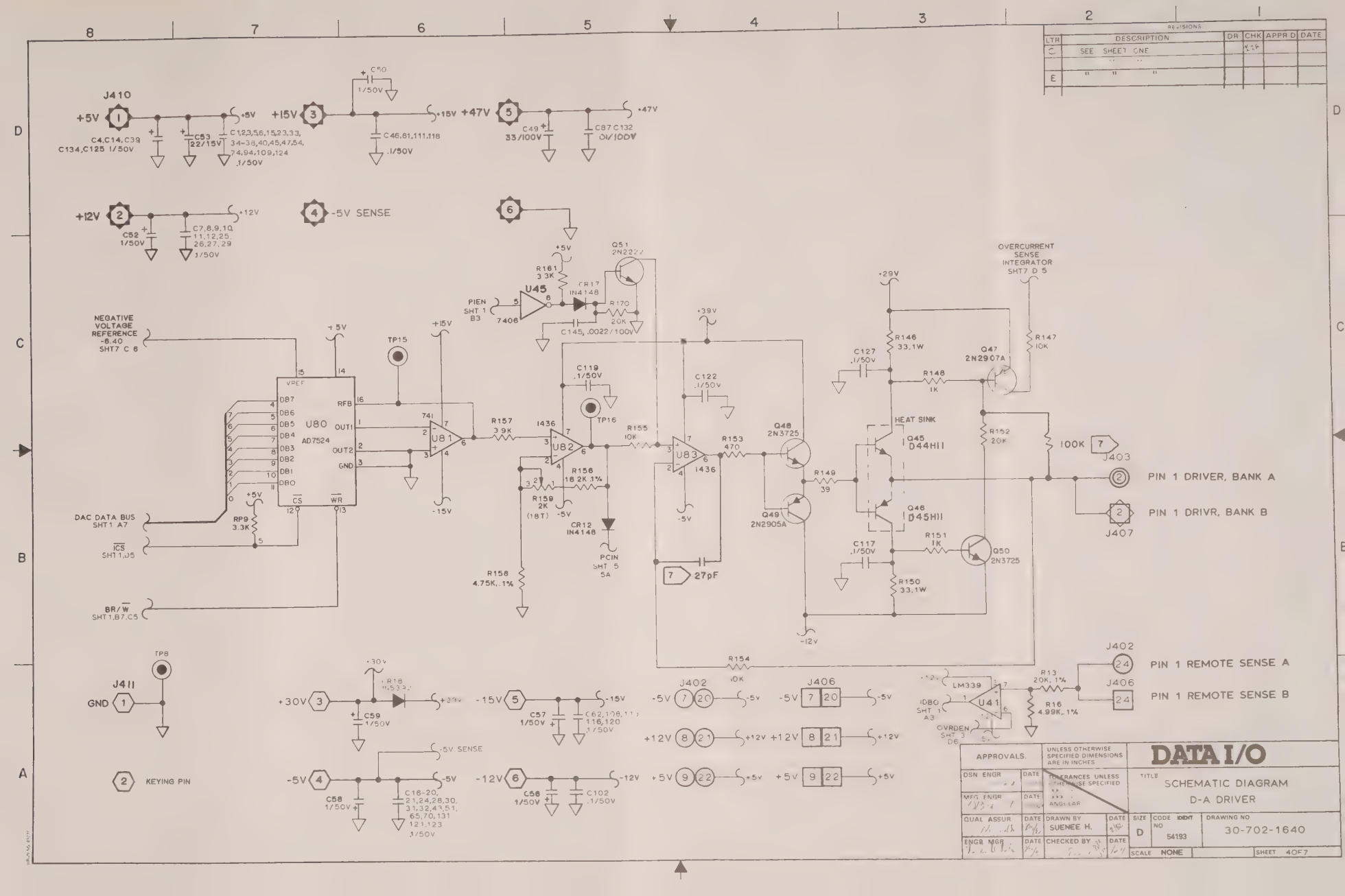
6 UNUSED GATES

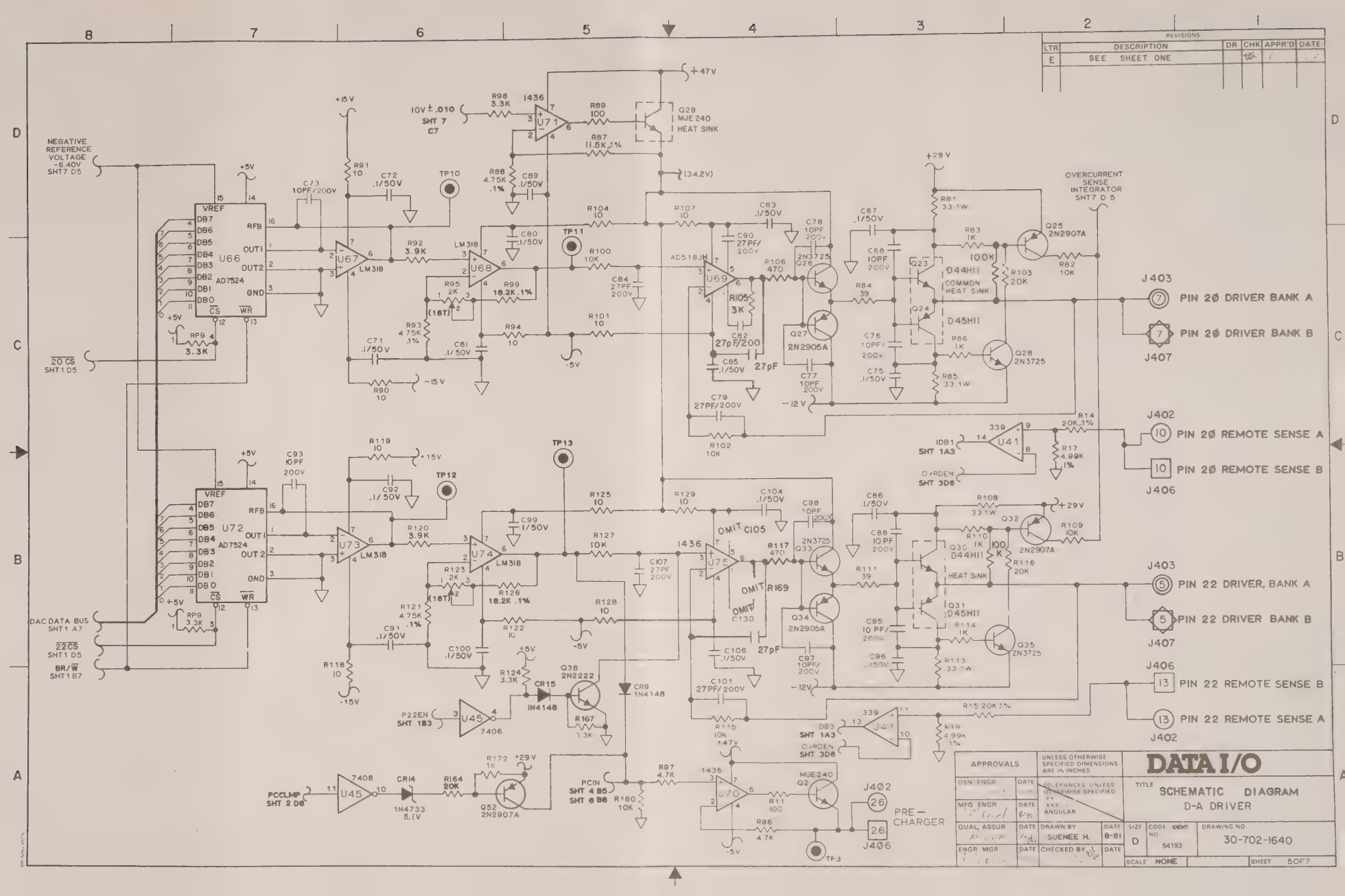
7. THIS REVISION REFLECTS CIRCUITRY EQUIVALENT TO 701-1673-001 REV 'A' ONLY.

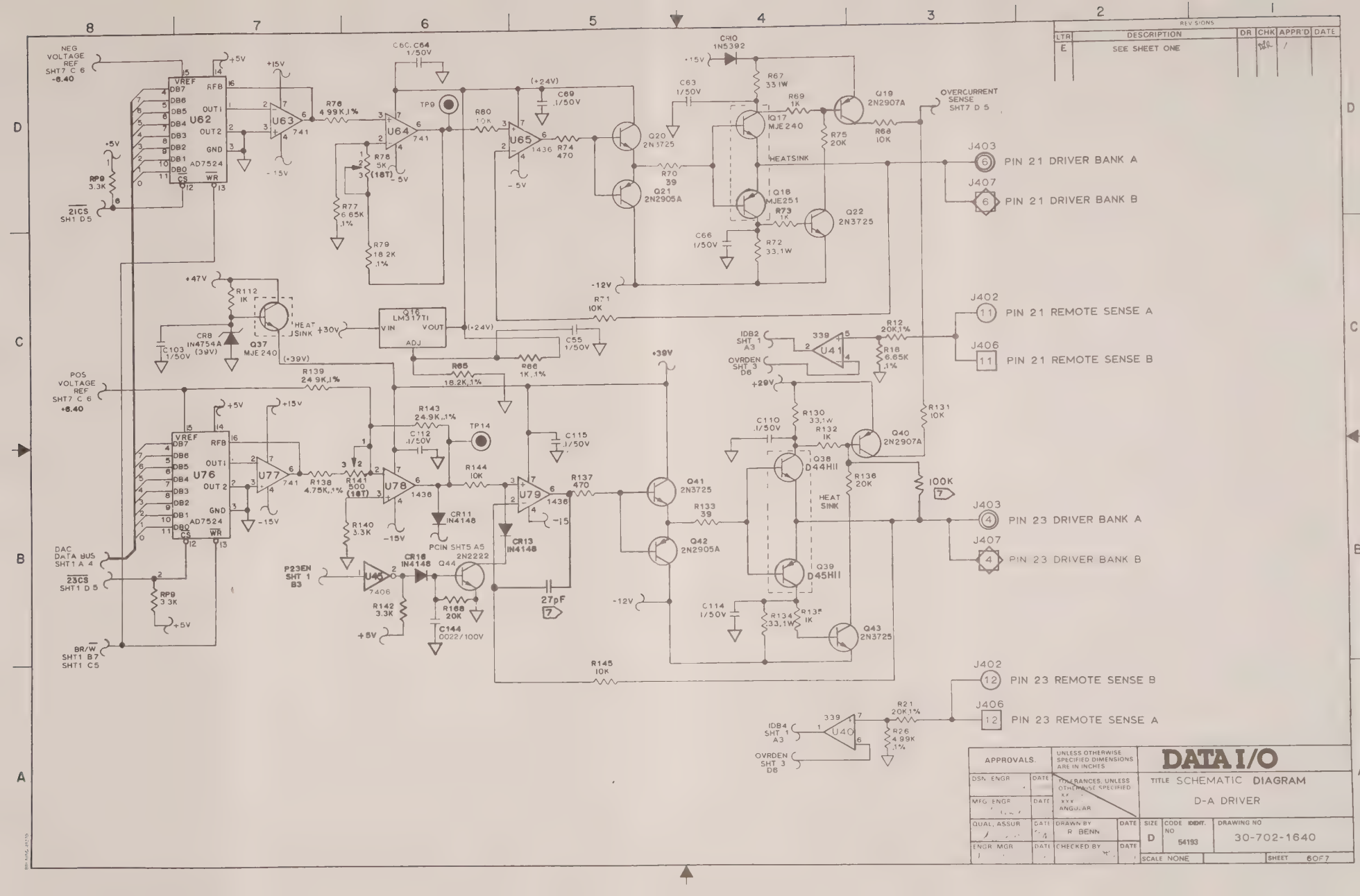
APPROVALS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
DSN ENGR	TOLERANCES UNLESS OTHERWISE SPECIFIED	TITLE SCHEMATIC DIAGRAM D-A DRIVER
MFG ENGR		
QUAL ASSUR	DRAWN BY R. BENN	SIZE D; CODE IDENT NO 54193; DRAWING NO 30-702-1640
ENGR MGR	CHECKED BY	SCALE NONE; SHEET 1 OF 7

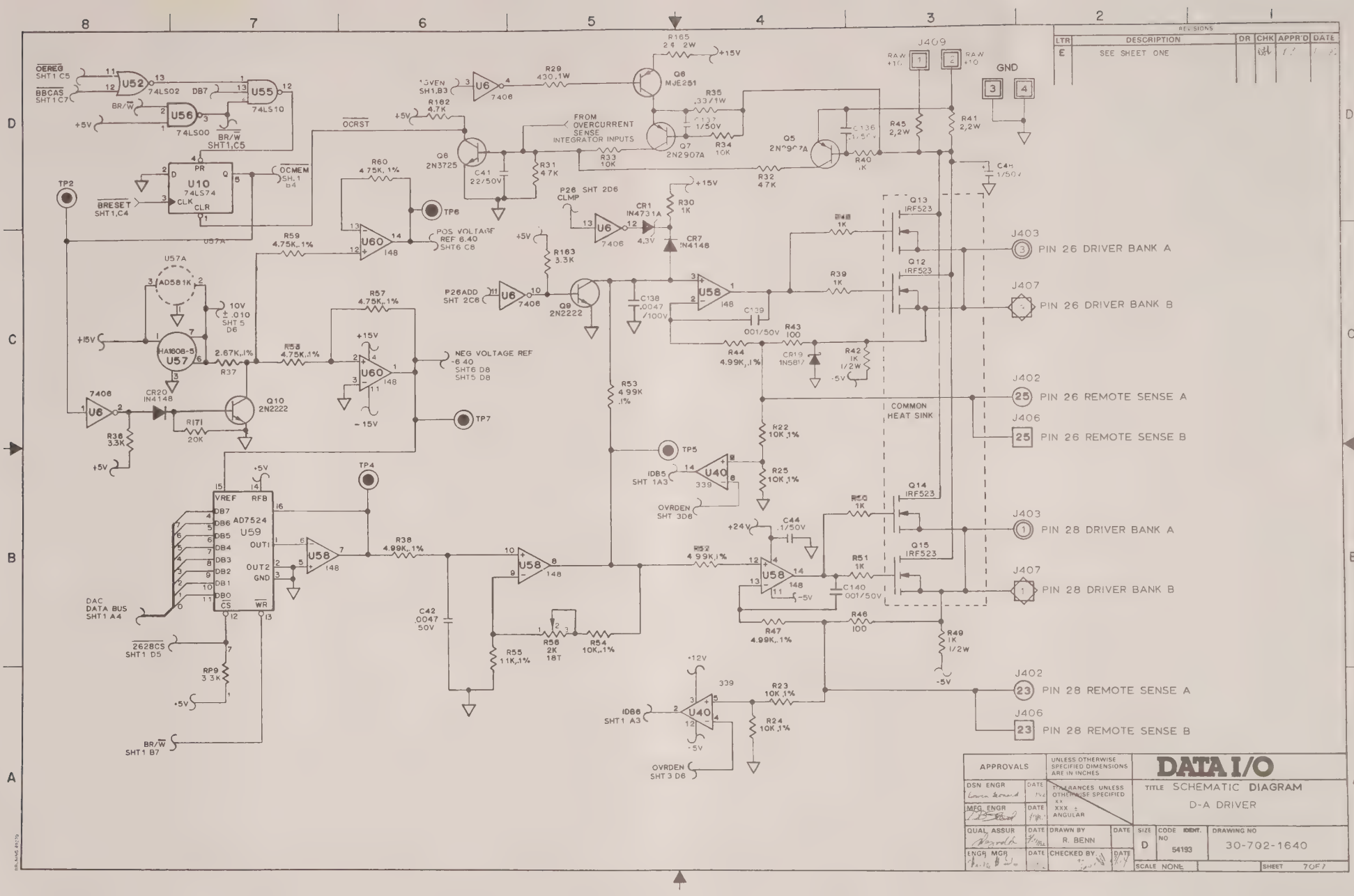

REVISIONS
LTR DESCRIPTION DR CHK APPR D DATE
SEE SHEET ONE
LOADLD SHT 1C5
RP8 3.3K +5V
U34 74C374
U42 74C374
U36 1K
U43 1K
PCCLMP SHT5, A7
P26 CLMP SHT 7,D5
SSEN
2N2907A Q3
+12V
R20 1K
R27 22
CR5 1N4148
R9 2.7K
CR4 1N4733A 5.1V
U45 7406
5.1V
1N4733A CR3
Q1 MJE 800
R8 470
R10 470
DIGITAL DATA BUS SHT1,A4 SHT2,A3
U40 339
P26ADD SHT7,C6
HORDB SHT 3D6
U39 339
U38 339
U37 339
-5V
IDB7 SHT1,A3
IDB6 SHT1,A3
IDB5 SHT1,A3
IDB4 SHT1,A3
IDB3 SHT1,A3
IDB2 SHT1,A3
IDB1 SHT1,A3
IDB0 SHT1,A3
LORDB SHT 3D6
U44
TID121
U35
TID121
LEDWR3 SHT1 C5
LEDWR2 SHT1,C5
LEDWR1 SHT1 C5
U7 74C374
7406
R4 150
R3 150
R2 150
R1 150
U2 150
U1 150
J408
LED10B
LED9B
LED8B
LED7B
LED6B
LED5B
LED4B
LED3B
LED2B
LED1B
LED10A
LED9A
J404
LED8A
LED7A
LED6A
LED5A
LED4A
LED3A
LED2A
LED1A
DIGITAL DATA BUS SHT1,A4 SHT2,C8
J406
J402
PIN 27 PGM
PIN 2 A12
PIN 24 A9
PIN 25 A8
PIN 3 A7
PIN 4 A6
PIN 5 A5
PIN 6 A4
PIN 7 A3
PIN 8 A2
PIN 9 A1
PIN 10 A0
APPROVALS
DSN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
DRAWN BY
CHECKED BY
DATA I/O
TITLE
SCHEMATIC DIAGRAM, D-A DRIVER
SIZE D
CODE NO 54193
DRAWING NO 30-702-1640
SCALE NONE
SHEET 2 OF 7

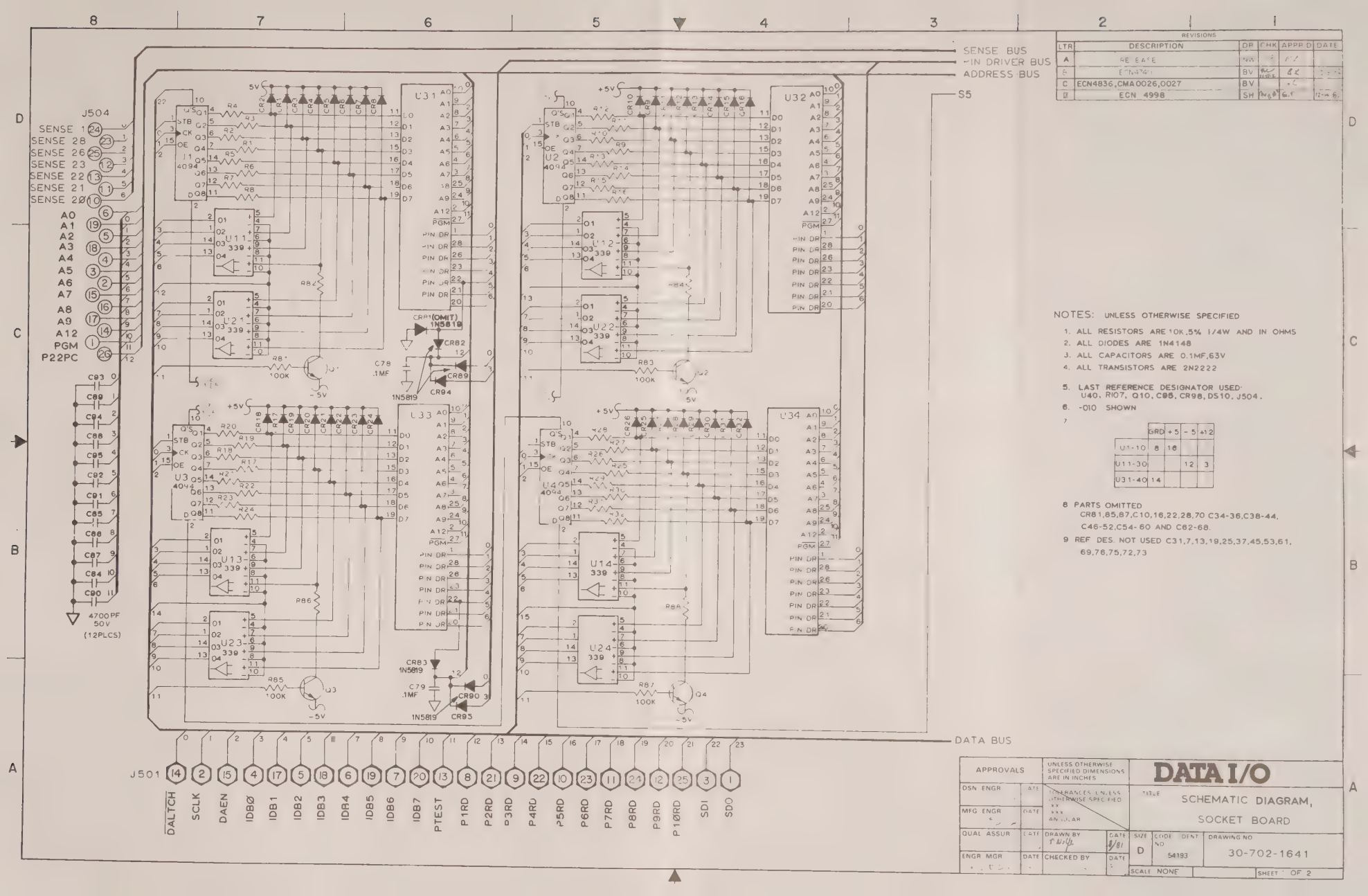

REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE
U15 74LS138
U11 74LS04
U12 74C374
U13 74LS138
U14 74LS138
U16 339
U17 339
U18 339
U19 339
U20 339
U21 339
U22
U23
U24
U25
U26
U27
U32
U33
MPQ3725
CDAC SHT 1, A4
OVRD
LOADRD
OVRDEN
PRRDEN SHT 1, D5
DIGITAL DATA BUS SHT 1, A4
J405
J401
P0RD
P19RD
P18RD
P17RD
P16RD
P15RD
P14RD
P13RD
P12RD
P11RD
P10RD
P9RD
P8RD
P7RD
P6RD
P5RD
P4RD
P3RD
P2RD
P1RD
PTEST
1N4148
DATA I/O
TITLE SCHEMATIC DIAGRAM
D-A DRIVER
DRAWING NO 30-702-1640
SIZE D
CODE IDENT. NO 54193
SCALE NONE
SHEET 3 OF 7
DRAWN BY R. BENN


REVISIONS
LTR DESCRIPTION DR CHK APPR D DATE
C SEE SHEET ONE
E " " "
J410
+5V
+15V
+47V
+12V
C4,C14,C39 C134,C125 1/50V
C53 22/15V
C123,56,15,23,33, 34-38,40,45,47,54, 74,94,109,124 .1/50V
C50 1/50V
C46,61,111,118 .1/50V
C49 33/100V
C87 C132 .01/100V
C52 1/50V
C7,8,9,10 11,12,25 26,27,29 1/50V
-5V SENSE
NEGATIVE VOLTAGE REFERENCE -6.40 SHT7 C 6
U80 AD7524
U81
U82
U83
U45 7406
PIEN SHT 1 B3
Q51 2N2222
R161 3.3K
CR17 IN4148
R170 20K
C145, .0022/100V
TP15
TP16
C119 .1/50V
C122 .1/50V
R157 3.9K
R155 10K
R153 470
R156 182K 1%
R159 2K (18T)
CR12 IN4148
PCIN SHT 5 5A
R158 4.75K, 1%
27pF
Q48 2N3725
Q49 2N2905A
OVERCURRENT SENSE INTEGRATOR SHT7 D 5
R146 33.1W
R147 10K
C127 .1/50V
Q47 2N2907A
R148 1K
HEAT SINK
Q45 D44H11
Q46 D45H11
R152 20K
100K
J403
PIN 1 DRIVER, BANK A
J407
PIN 1 DRIVR, BANK B
R149 39
C117 .1/50V
R151 1K
Q50 2N3725
R150 33.1W
DAC DATA BUS SHT1 A7
CS SHT 1,D5
BR/W SHT 1,B7,C5
RP9 3.3K
R154 10K
J411
GND
TP8
KEYING PIN
+30V
-15V
C59 1/50V
C57 1/50V
C62,108,111, 116,120 .1/50V
C58 1/50V
C16-20, 21,24,28,30, 31,32,43,51, 65,70,131 121,123 .1/50V
C102 .1/50V
J402
J406
-5V
+12V
+5V
LM339
U41
IDBO SHT 1 A3
OVRDEN SHT 3 D6
R13 20K, 1%
R16 4.99K, 1%
J402
PIN 1 REMOTE SENSE A
J406
PIN 1 REMOTE SENSE B
APPROVALS
DSN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
DRAWN BY SUENEE H.
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM D-A DRIVER
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-702-1640
SCALE NONE
SHEET 4OF7


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE
NEGATIVE REFERENCE VOLTAGE -6.40V SHT7 D5
+47V
+15V
+5V
+29V
-15V
-5V
-12V
10V ± .010 SHT 7 C7
Q29 MJE 240 HEAT SINK
(34.2V)
TP10
TP11
TP12
TP13
U66 AD7524
U67 LM318
U68 LM318
U69 AD518JH
U70
U71 1436
U72 AD7524
U73 LM318
U74 LM318
U45 7406
U41 339
OVERCURRENT SENSE INTEGRATOR SHT7 D 5
COMMON HEAT SINK
OMIT C105
OMIT R169
OMIT C130
20 CS SHT1 D5
22 CS SHT1 D5
BR/W SHT1 B7
DAC DATA BUS SHT1 A7
P22EN SHT 1B3
PCCLMP SHT 2 D8
PCIN SHT 4 B5 SHT 6 B6
IDB1 SHT 1A3
DB3 SHT 1A3
O/RDEN SHT 3D6
J403 PIN 20 DRIVER BANK A
J407 PIN 20 DRIVER BANK B
J402 PIN 20 REMOTE SENSE A
J406 PIN 20 REMOTE SENSE B
J403 PIN 22 DRIVER, BANK A
J407 PIN 22 DRIVER BANK B
J406 PIN 22 REMOTE SENSE B
J402 PIN 22 REMOTE SENSE A
J402 J406 PRE-CHARGER
APPROVALS
DSN ENGR
MFG ENGR
QUAL. ASSUR
ENGR MGR
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
XX ± .01
XXX ± .005
ANGULAR
DATA I/O
TITLE SCHEMATIC DIAGRAM D-A DRIVER
DRAWN BY SUENEE H. 8-81
CHECKED BY
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-702-1640
SCALE NONE
SHEET 5OF7


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE
NEG VOLTAGE REF SHT7 C 6 -8.40
POS VOLTAGE REF SHT7 C 6 +8.40
U62 AD7524
U63 741
U64 741
U65 1436
U76 AD7524
U77 741
U78 1436
U79 1436
U45 7406
U41 339
U40 339
Q16 LM317TI
Q37 MJE240
Q17 MJE240
Q18 MJE251
Q19 2N2907A
Q20 2N3725
Q21 2N2905A
Q22 2N3725
Q38 D44H11
Q39 D45H11
Q40 2N2907A
Q41 2N3725
Q42 2N2905A
Q43 2N3725
Q44 2N2222
CR8 IN4754A (39V)
CR10 1N5392
CR11 IN4148
CR13 IN4148
CR16 IN4148
HEAT SINK
J403 6 PIN 21 DRIVER BANK A
J407 6 PIN 21 DRIVER BANK B
J402 11 PIN 21 REMOTE SENSE A
J406 11 PIN 21 REMOTE SENSE B
J403 4 PIN 23 DRIVER BANK A
J407 4 PIN 23 DRIVER BANK B
J402 12 PIN 23 REMOTE SENSE B
J406 12 PIN 23 REMOTE SENSE A
OVERCURRENT SENSE SHT7 D 5
2ICS SHT1 D5
23CS SHT1 D5
DAC DATA BUS SHT1 A 4
BR/W SHT1 B7 SHT1 C5
P23EN SHT 1 B3
IDB2 SHT 1 A3
IDB4 SHT 1 A3
OVRDEN SHT 3 D6
PCIN SHT5 A5
+47V +30V (+24V) -12V +39V +29V +5V +15V -15V -5V
R67 33.1W
R69 1K
R68 10K
R75 20K
R70 39
R73 1K
R72 33.1W
R71 10K
R74 470
R76 4.99K,1%
R77 6.65K,1%
R78 5K (18T)
R79 18.2K,1%
R80 10K
R112 1K
R65 18.2K,1%
R66 1K,1%
R139 24.9K,1%
R143 24.9K,1%
R141 500 (18T)
R138 4.75K,1%
R140 3.3K
R142 3.3K
R144 10K
R137 470
R145 10K
R130 33.1W
R132 1K
R131 10K
R136 20K
R133 39
R134 33.1W
R135 1K
R12 20K,1%
R18 6.65K,1%
R21 20K,1%
R26 4.99K,1%
RP9 3.3K
C60, C64 1/50V
C69 .1/50V
C63 1/50V
C66 1/50V
C55 1/50V
C103 1/50V
C112 .1/50V
C115 .1/50V
C110 .1/50V
C114 1/50V
C144 .0022/100V
27pF
100K
R168 20K
TP9
TP14
APPROVALS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES, UNLESS OTHERWISE SPECIFIED .XX ±.01 .XXX ±.005 ANGULAR
DSN ENGR
MFG ENGR
QUAL. ASSUR
ENGR MGR
DRAWN BY R BENN
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM
D-A DRIVER
SIZE D
CODE IDENT. NO 54193
DRAWING NO 30-702-1640
SCALE NONE
SHEET 6OF7


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE
J409
RAW +10
GND
R165 24 2W
+15V
Q6 MJE251
R35 .33/1W
C137 1/50V
R34 10K
Q7 2N2907A
Q5 2N2907A
C136 .1/50V
R45 2,2W
R41 2,2W
C45 1/50V
R40 1K
R32 47K
R33 10K
FROM OVERCURRENT SENSE INTEGRATOR INPUTS
R29 430,1W
U6 7406
R162 4.7K
Q8 2N3725
C41 22/50V
R31 47K
OCRST
OCMEM SH.1 B4
BRESET SHT1,C4
BR/W SHT1,C5
U10 74LS74
U52 74LS02
U55 74LS10
U56 74LS00
DB7
TP2
R60 4.75K,.1%
U60 148
TP6
POS VOLTAGE REF 6.40 SHT6 C8
R59 4.75K,.1%
U57A AD581K
10V ±.010 SHT 5 D6
+15V
HA1608-5 U57
2.67K,.1%
R37
R58 4.75K,.1%
R57 4.75K,.1%
NEG VOLTAGE REF -6.40 SHT6 D8 SHT5 D8
TP7
CR20 IN4148
Q10 2N2222
R171 20K
R36 3.3K
+5V
-15V
P26 SHT 2D6 CLMP
CR1 IN4731A 4.3V
R30 1K
CR7 IN4148
R163 3.3K
P26ADD SHT 2C6
Q9 2N2222
C138 .0047 /100V
U58 148
C139 .001/50V
R43 100
R44 4.99K,.1%
CR19 1N5817
R42 1K 1/2W
-5V
R53 4.99K .1%
R22 10K,1%
R25 10K,1%
TP5
IDB5 SHT 1A3
U40 339
OVRDEN SHT 3D6
COMMON HEAT SINK
Q13 IRF523
Q12 IRF523
Q14 IRF523
Q15 IRF523
R48 1K
R39 1K
R50 1K
R51 1K
J403 PIN 26 DRIVER BANK A
J407 PIN 26 DRIVER BANK B
J402 PIN 26 REMOTE SENSE A
J406 PIN 26 REMOTE SENSE B
J403 PIN 28 DRIVER BANK A
J407 PIN 28 DRIVER BANK B
J402 PIN 28 REMOTE SENSE A
J406 PIN 28 REMOTE SENSE B
TP4
AD7524 U59
VREF RFB DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 CS WR OUT1 OUT2 GND
DAC DATA BUS SHT1 A4
2628CS SHT1 D5
RP9 3.3K
BR/W SHT1 B7
R38 4.99K,.1%
C42 .0047 50V
R55 11K,1%
R56 2K 18T
R54 10K,.1%
C44 .1/50V
+24V
R52 4.99K,.1%
C140 .001/50V
R47 4.99K,.1%
R46 100
R49 1K 1/2W
+12V
IDB6 SHT1 A3
R23 10K,1%
R24 10K,1%
OVRDEN SHT 3 D6
APPROVALS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
DSN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
DRAWN BY R. BENN
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM
D-A DRIVER
SIZE D
CODE IDENT. NO 54193
DRAWING NO 30-702-1640
SCALE NONE
SHEET 7OF7



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	WK	[illegible]	[illegible]	[illegible]
B	ECN4794	BV	[illegible]	[illegible]	[illegible]
C	ECN4836,CMA0026,0027	BV	[illegible]	[illegible]	[illegible]
D	ECN 4998	SH	[illegible]	[illegible]	[illegible]

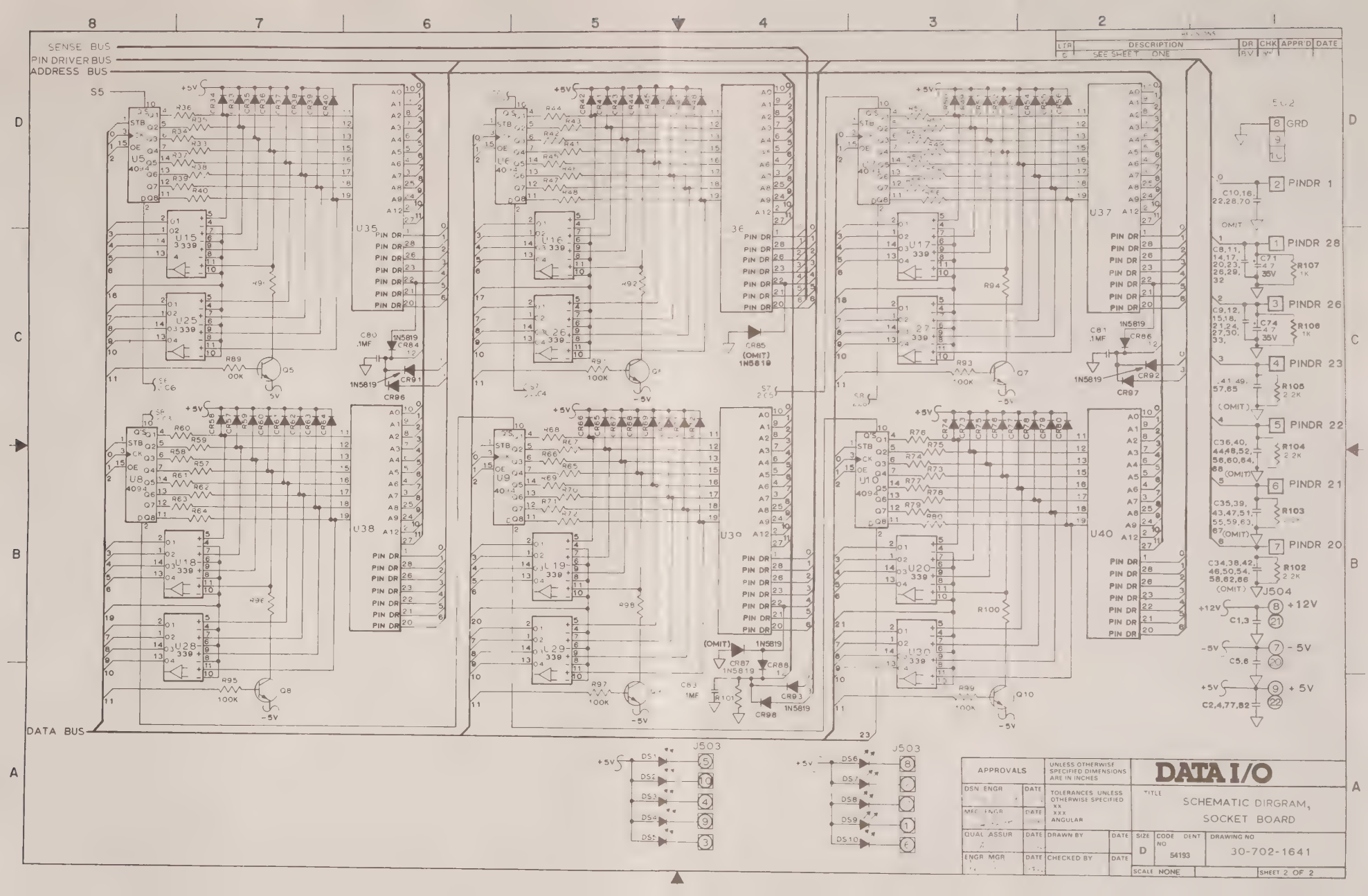
NOTES: UNLESS OTHERWISE SPECIFIED

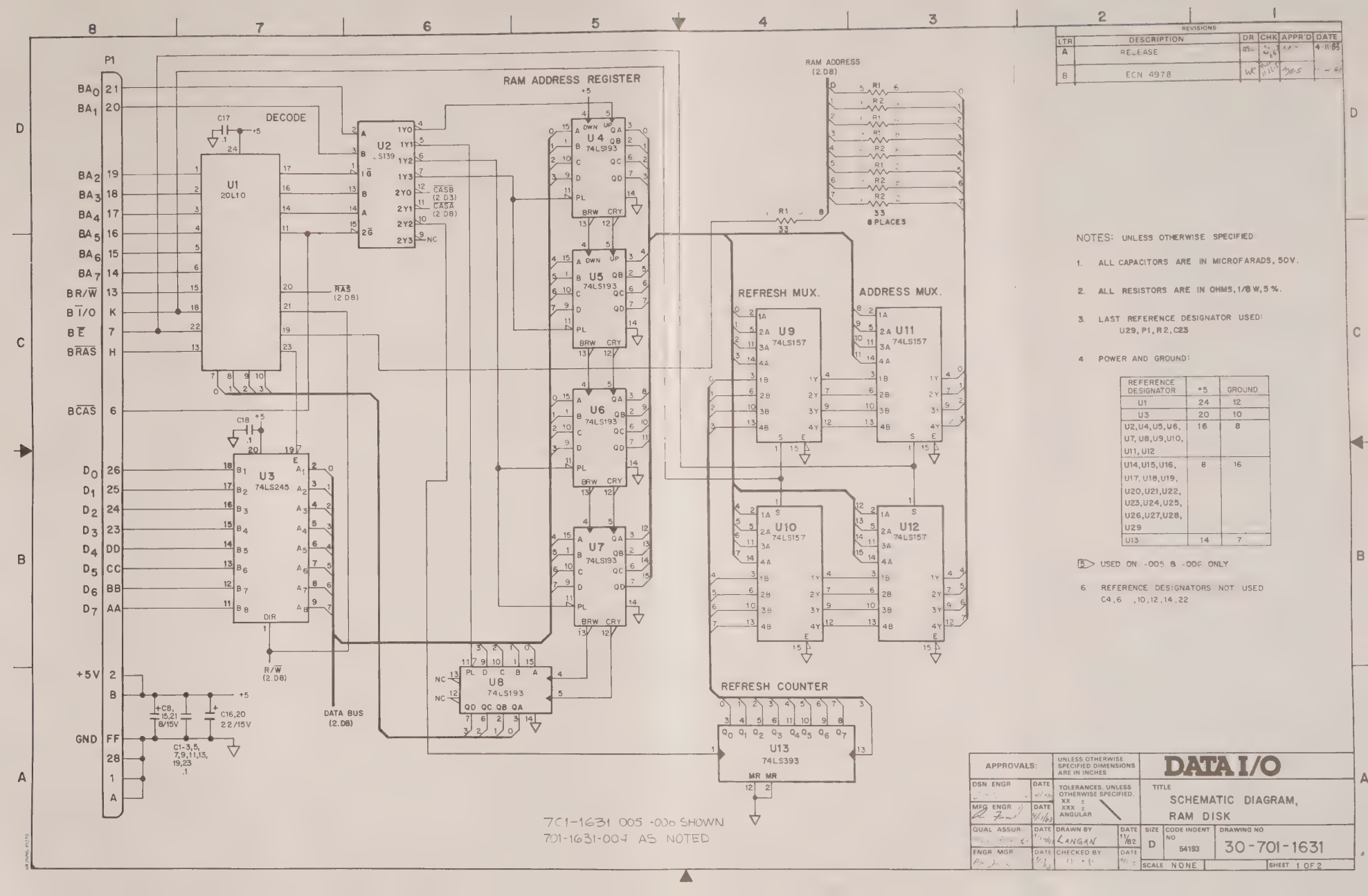
1. ALL RESISTORS ARE 10K,5% 1/4W AND IN OHMS
2. ALL DIODES ARE 1N4148
3. ALL CAPACITORS ARE 0.1MF,63V
4. ALL TRANSISTORS ARE 2N2222
5. LAST REFERENCE DESIGNATOR USED: U40, R107, Q10, C85, CR98, DS10, J504.
6. -010 SHOWN
7.

	GRD	+5	-5	+12
U1-10	8	16		
U11-30			12	3
U31-40	14			

8. PARTS OMITTED CR81,85,87,C10,16,22,28,70 C34-36,C38-44, C46-52,C54-60 AND C62-68.
9. REF DES. NOT USED C31,7,13,19,25,37,45,53,61, 69,76,75,72,73

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED: XX ±.XX ±.XXX ANGULAR	TITLE: SCHEMATIC DIAGRAM, SOCKET BOARD	
MFG ENGR	DATE			
QUAL ASSUR	DATE	DRAWN BY: [illegible] DATE: 8/81	SIZE: D	CODE IDENT NO: 54193
ENGR MGR	DATE	CHECKED BY	DATE	DRAWING NO: 30-702-1641
			SCALE: NONE	SHEET 1 OF 2


SENSE BUS
PIN DRIVER BUS
ADDRESS BUS
DATA BUS
S5
U5
U8
U15
U16
U17
U18
U19
U20
U25
U26
U28
U29
U30
U35
U37
U38
U40
J503
J504
GRD
PINDR 1
PINDR 28
PINDR 26
PINDR 23
PINDR 22
PINDR 21
PINDR 20
+12V
-5V
+5V
DESCRIPTION
SEE SHEET ONE
APPROVALS
DSN ENGR
QUAL ASSUR
ENGR MGR
DRAWN BY
CHECKED BY
DATA I/O
SCHEMATIC DIRGRAM, SOCKET BOARD
DRAWING NO 30-702-1641
SHEET 2 OF 2



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE				4-11-83
B	ECN 4978	WR			1-6-84

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS, 50V.
2. ALL RESISTORS ARE IN OHMS, 1/8 W, 5 %.
3. LAST REFERENCE DESIGNATOR USED: U29, P1, R2, C23
4. POWER AND GROUND:

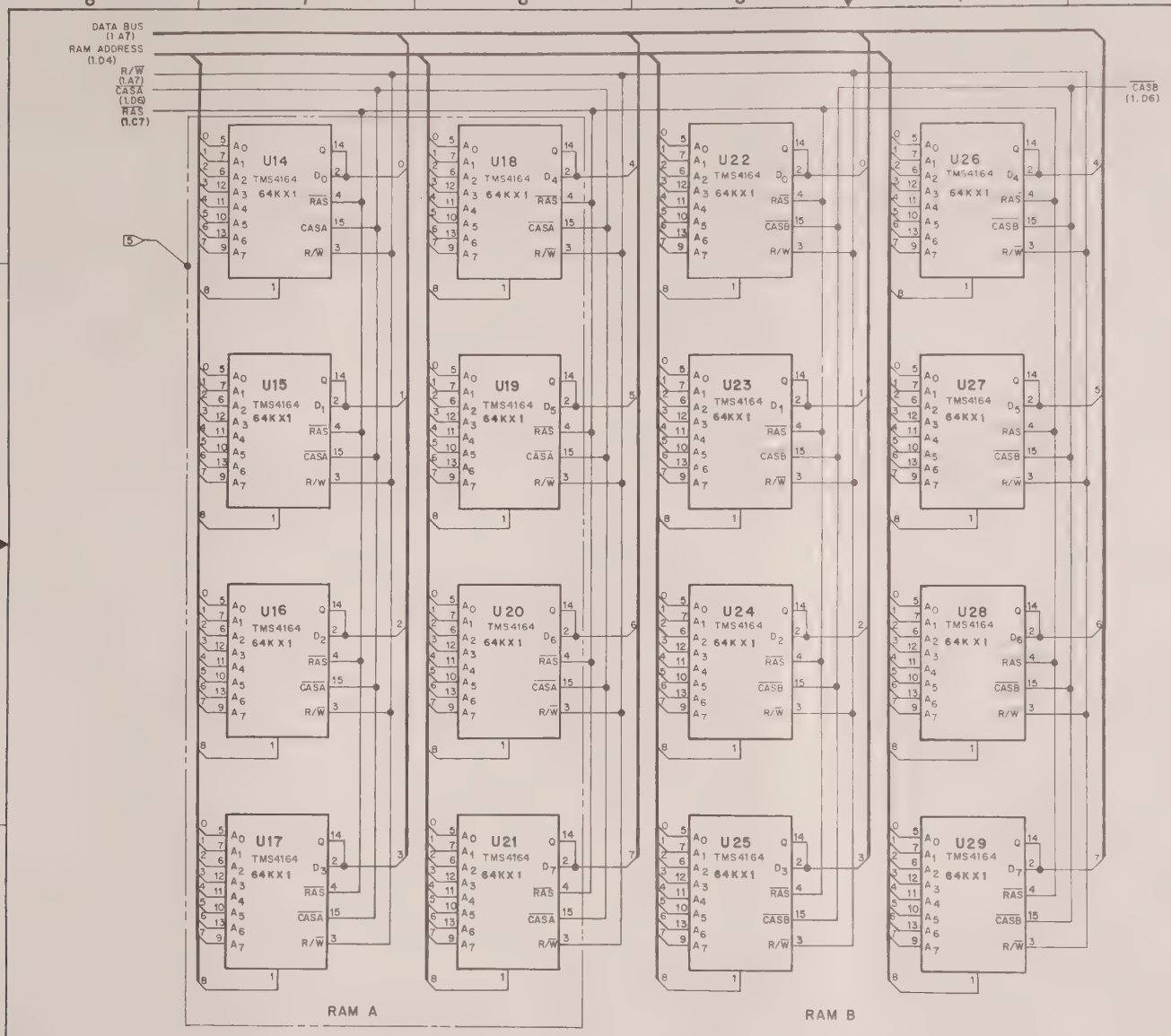
REFERENCE DESIGNATOR	+5	GROUND
U1	24	12
U3	20	10
U2,U4,U5,U6, U7, U8,U9,U10, U11, U12	16	8
U14,U15,U16, U17, U18,U19, U20,U21,U22, U23,U24,U25, U26,U27,U28, U29	8	16
U13	14	7

5 USED ON -005 & -006 ONLY

6. REFERENCE DESIGNATORS NOT USED C4,6 ,10,12,14,22

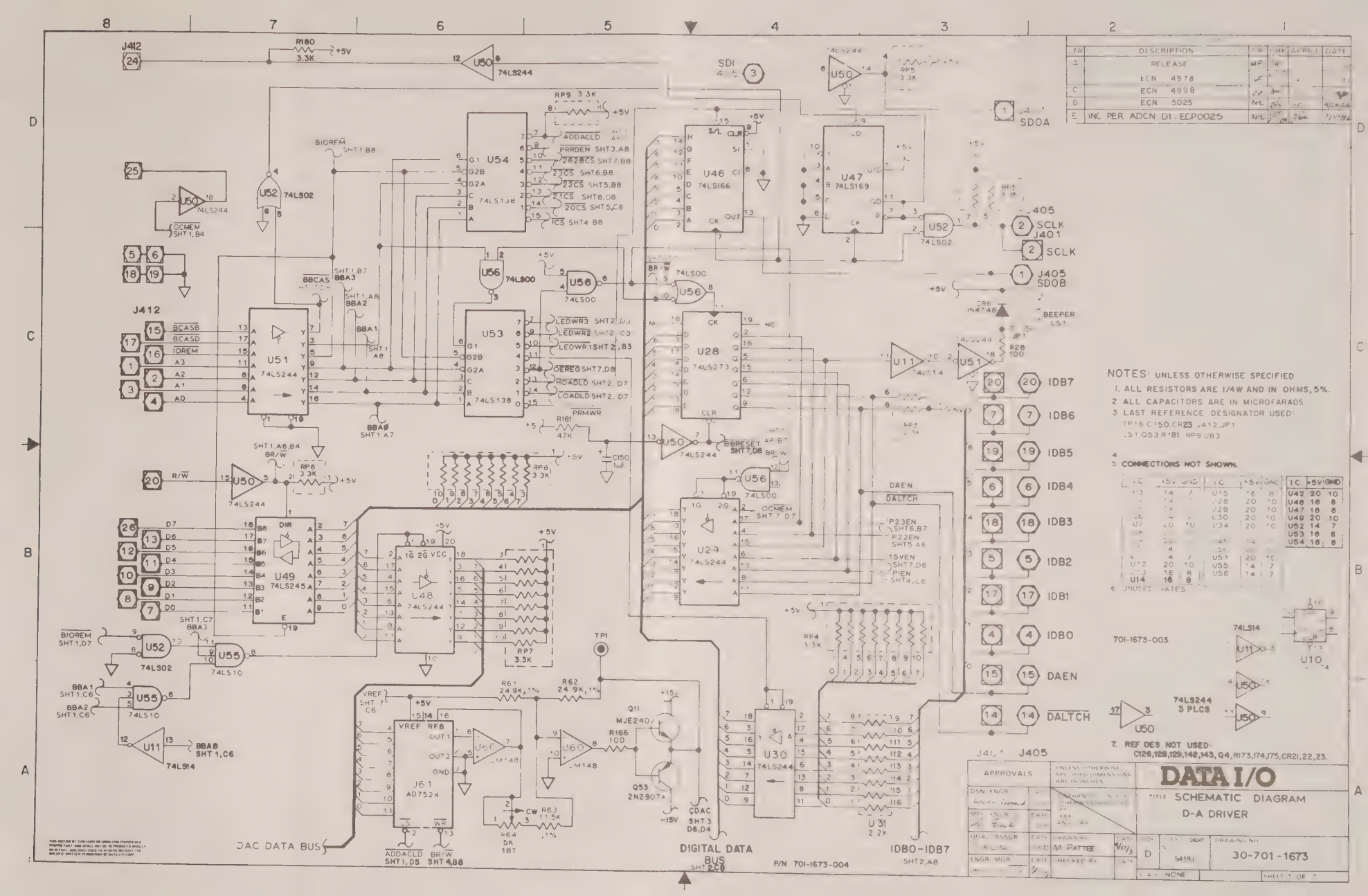
7C1-1631 005 -006 SHOWN
701-1631-004 AS NOTED

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED. XX ± XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, RAM DISK	
MFG ENGR	DATE			
QUAL ASSUR	DATE	DRAWN BY LANGAN	DATE 11/82	SIZE D / CODE INDENT NO 54193 / DRAWING NO 30-701-1631
ENGR MGR	DATE	CHECKED BY	DATE	SCALE NONE / SHEET 1 OF 2



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	SEE SHEET ONE				
B	SEE SHEET ONE				

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR / DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED. XX ± XXX ± ANGULAR	TITLE: SCHEMATIC DIAGRAM, RAM DISK	
MFG. ENGR / DATE			
QUAL ASSUR / DATE	DRAWN BY: CANGAN / DATE: 11/82	SIZE: D	CODE IDENT NO: 54193
ENGR MGR / DATE	CHECKED BY / DATE	DRAWING NO: 30-701-1631	
		SCALE: NONE	SHEET 2 OF 2



LTR	DESCRIPTION	BY	CHK	APPD	DATE
A	RELEASE	MP			
B	ECN 4978				
C	ECN 4998				
D	ECN 5025				
E	INC PER ADCN D1, ECP0025				

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS
3. LAST REFERENCE DESIGNATOR USED: TP16 C150 CR23 J412 JP1 LS1 Q53 R181 RP9 U83
4.
5. CONNECTIONS NOT SHOWN.

IC	+5V	GND
U42	20	10
U46	16	8
U47	16	8
U49	20	10
U52	14	7
U53	16	8
U54	16	8

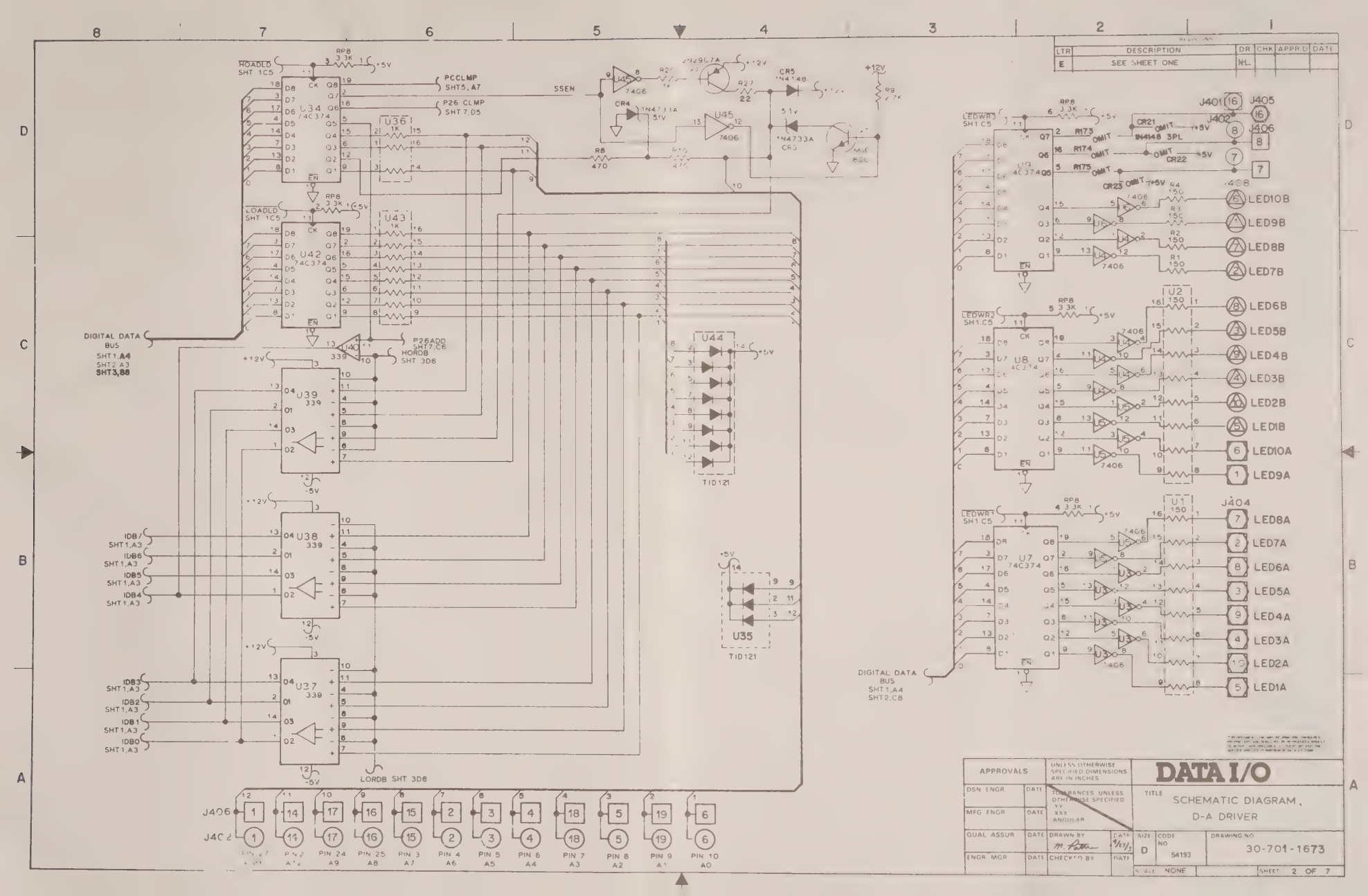
6. UNUSED GATES

IC	+5V	GND
U13	14	7
U14	16	8
U15	*6	8
U28	20	*0
U29	20	10
U30	20	10
U34	20	*0
U51	20	*0
U55	14	7
U56	14	7

7. REF DES NOT USED: C126,128,129,142,143, Q4, R173,174,175, CR21,22,23.

J40* J405

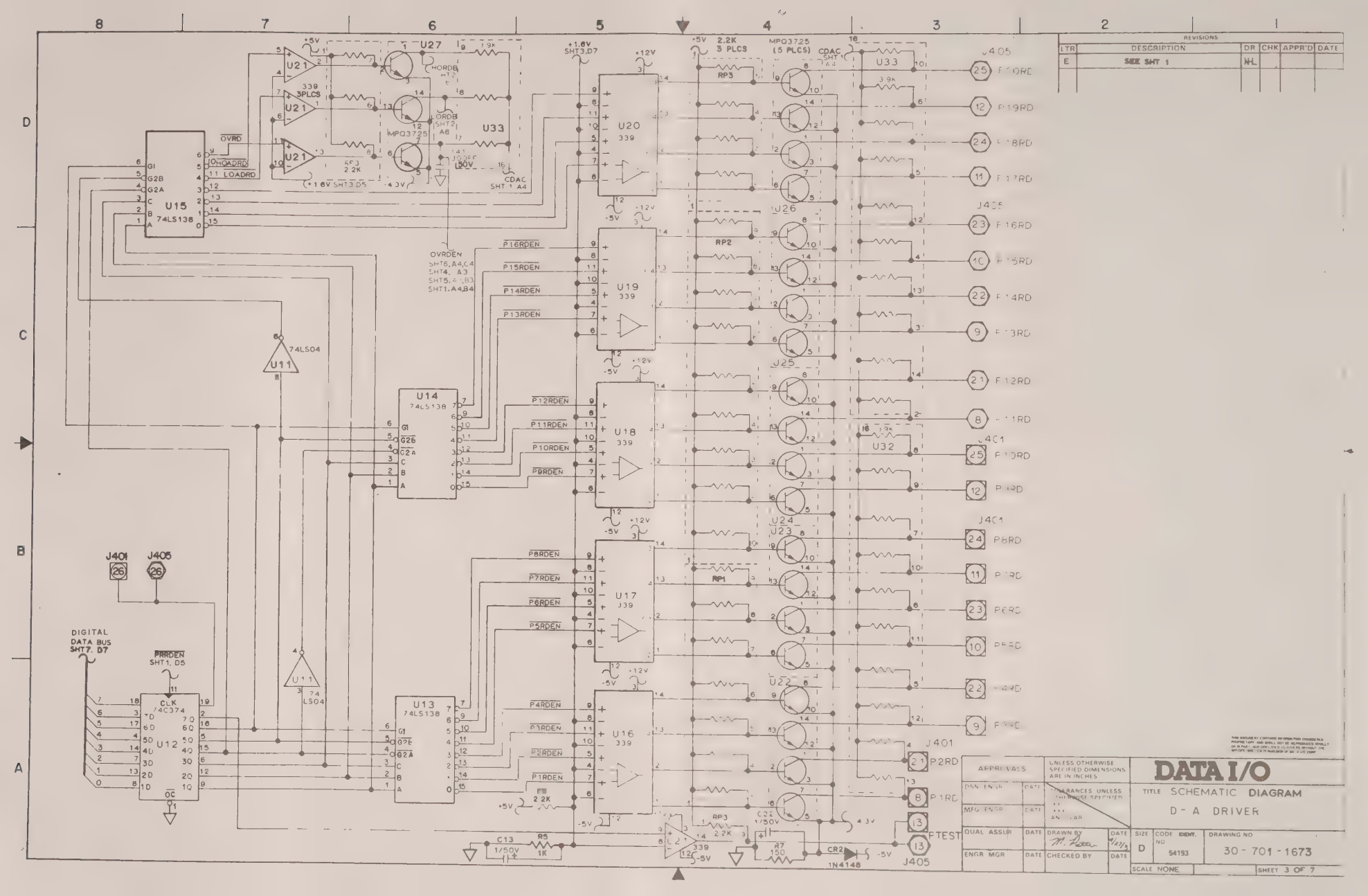
APPROVALS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
DSN ENGR		TITLE SCHEMATIC DIAGRAM D-A DRIVER
MFG ENGR		
QUAL ASSUR		
ENGR MGR	DRAWN M PATTEE	SIZE D
	CHECKED BY	DRAWING NO 30-701-1673
		SCALE NONE
		SHEET 1 OF 2

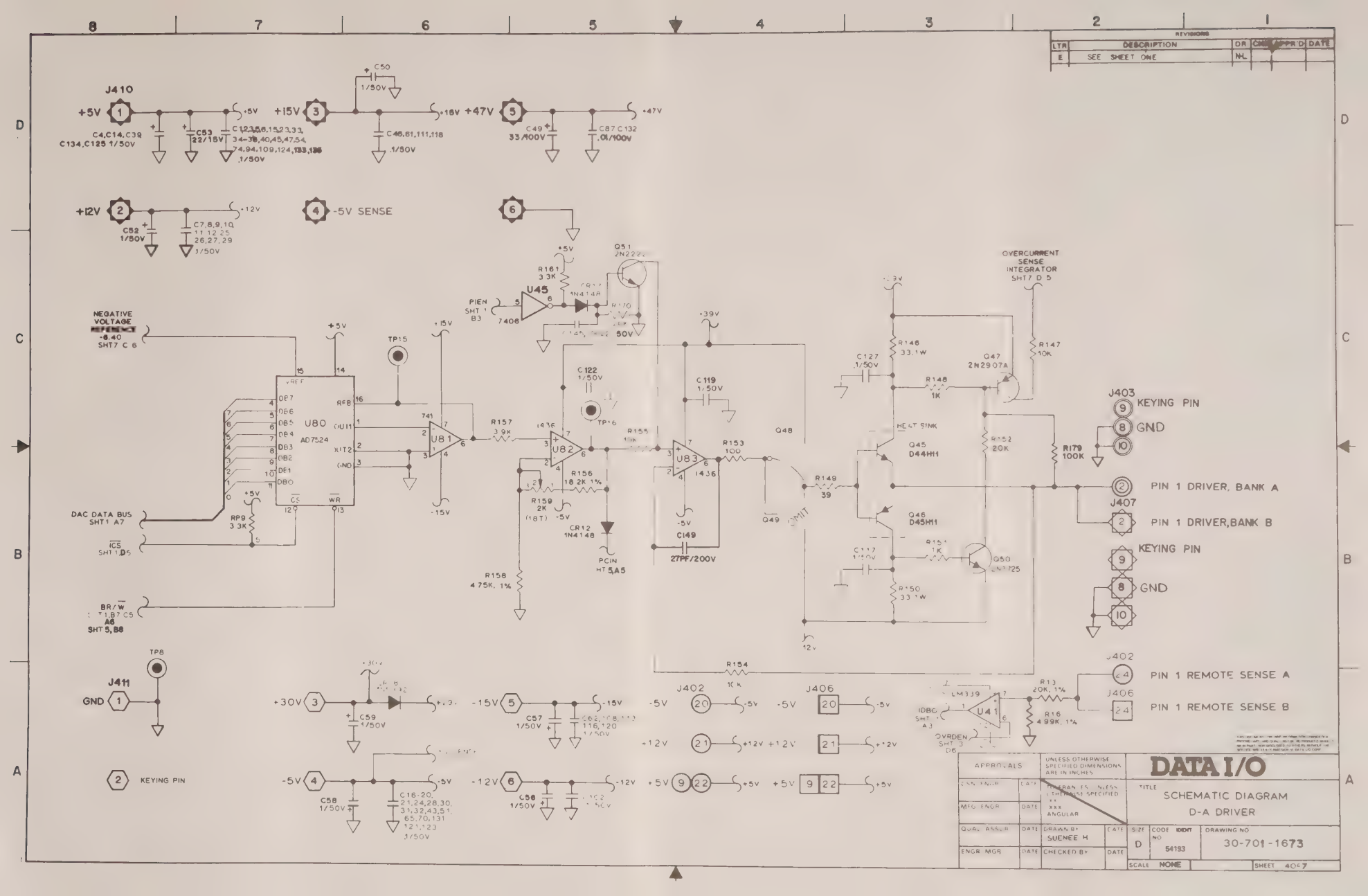


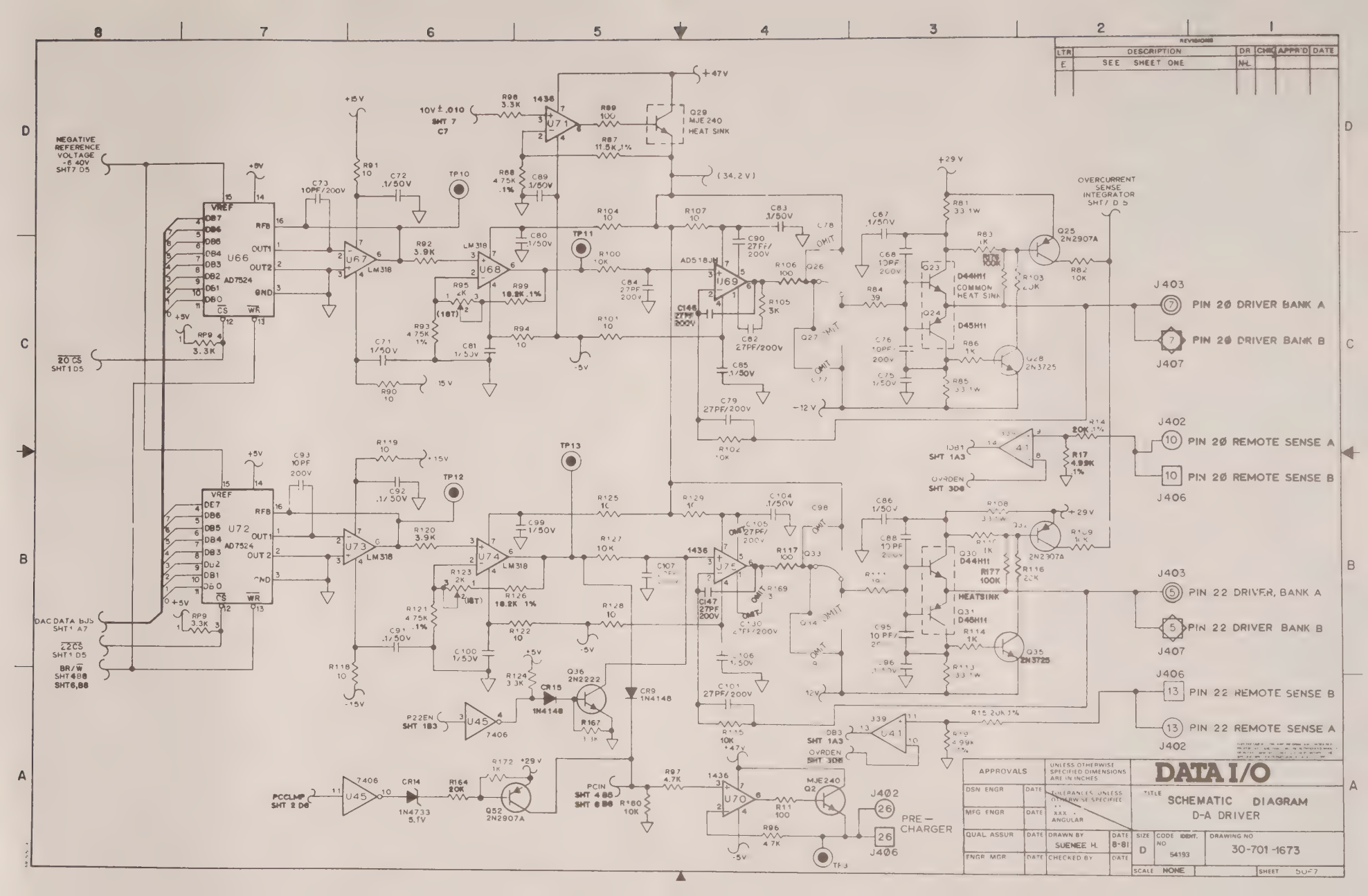
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
E	SEE SHEET ONE	NL			

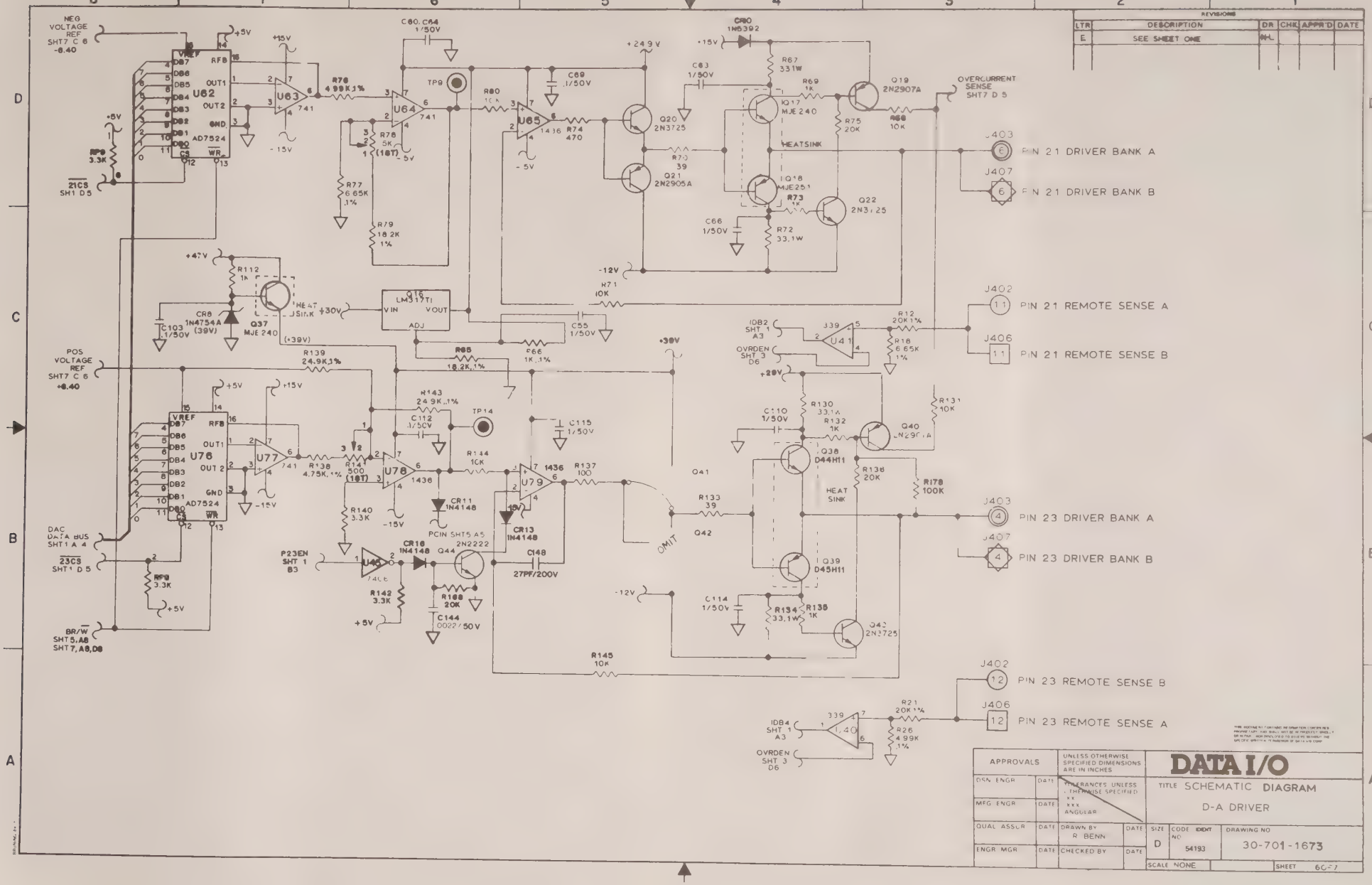
APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED .YY .XXX ANGULAR	TITLE SCHEMATIC DIAGRAM, D-A DRIVER	
MFG ENGR	DATE			
QUAL ASSUR	DATE	DRAWN BY M. Peterson DATE 9/27/83	SIZE D	CODE NO 54193
ENGR MGR	DATE	CHECKED BY	SCALE NONE	SHEET 2 OF 7

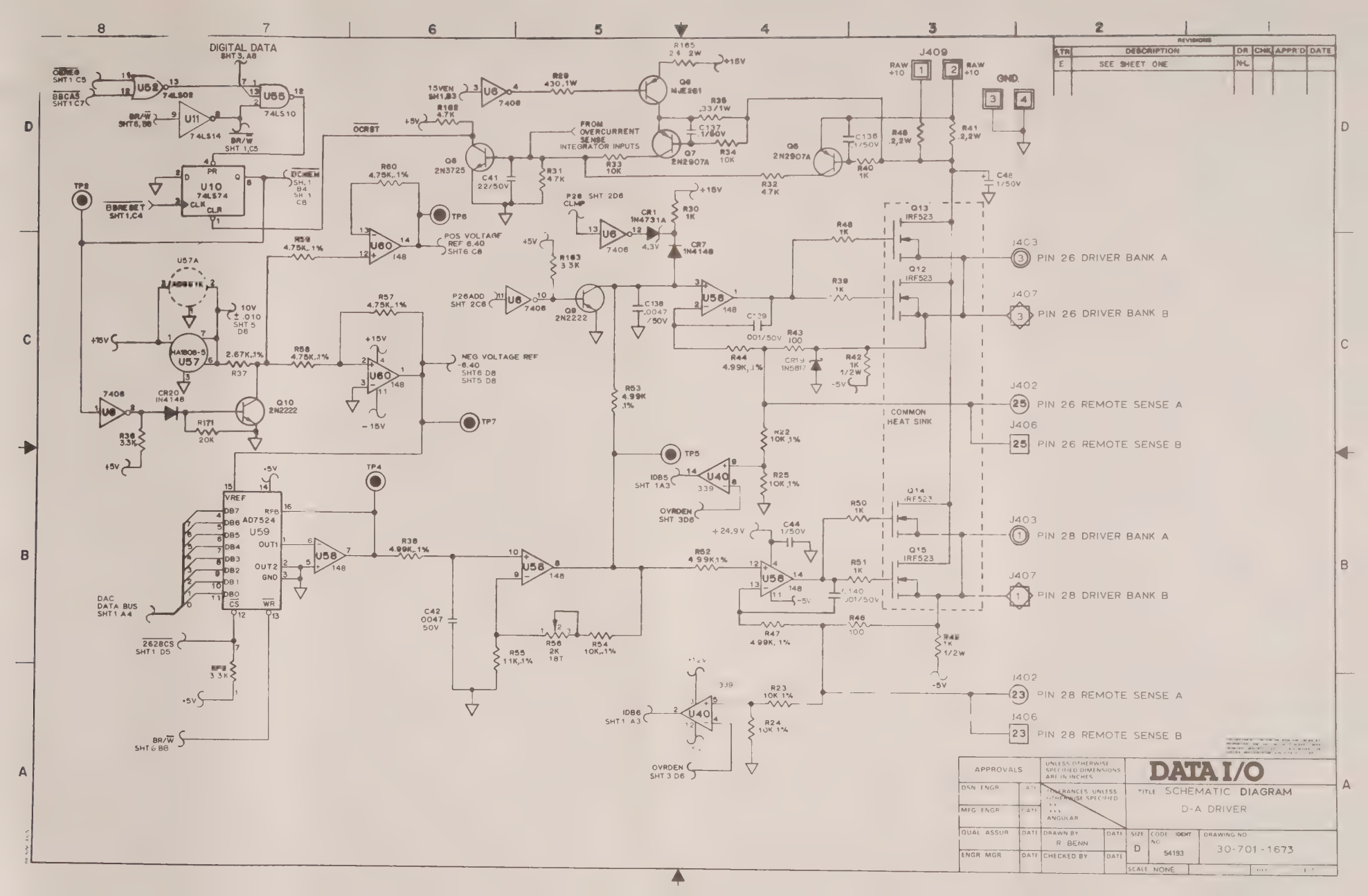
DRAWING NO 30-701-1673


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHT 1 NL
U15 74LS138
U14 74LS138
U13 74LS138
U12 CLK 74C374
U11 74LS04
U20 339
U19 339
U18 339
U17 339
U16 339
U21 339 3PLCS
U27 MPQ3725
U33
U26
U25
U24
U23
U22
U32
MPQ3725 (5 PLCS)
2.2K 3 PLCS
RP3
RP2
RP1
OVRD
LOADRD
OVRDEN
DIGITAL DATA BUS SHT7. D7
PRRDEN SHT1. D5
J401
J405
J401
J405
P16RDEN
P15RDEN
P14RDEN
P13RDEN
P12RDEN
P11RDEN
P10RDEN
P9RDEN
P8RDEN
P7RDEN
P6RDEN
P5RDEN
P4RDEN
P3RDEN
P2RDEN
P1RDEN
P2RD
P1RD
FTEST
1N4148
DATA I/O
TITLE SCHEMATIC DIAGRAM
D-A DRIVER
DRAWING NO 30-701-1673
SIZE D
CODE IDENT. NO 54193
SCALE NONE
SHEET 3 OF 7


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE NL
J410
+5V
+15V
+47V
+12V
-5V SENSE
C4,C14,C39 C134,C125 1/50V
C53 22/15V
C46,61,111,118 .1/50V
C49 33/100V
C87 C132 .01/100V
C52 1/50V
C7,8,9,10 11,12,25 26,27,29 .1/50V
C50 1/50V
NEGATIVE VOLTAGE REFERENCE -8.40 SHT7 C 6
U80 AD7524
U81
U82
U83
U45 7406
Q51 2N2222
Q47 2N2907A
Q45 D44H11
Q46 D45H11
Q48
Q49 OMIT
Q50 LM7725
OVERCURRENT SENSE INTEGRATOR SHT7 D 5
HEAT SINK
TP15
TP16
TP8
R161 3.3K
R157 3.9K
R156 18.2K 1%
R159 2K (18T)
R158 4.75K, 1%
R155 10K
R153 100
R154 10K
R146 33,1W
R147 10K
R148 1K
R152 20K
R179 100K
R149 39
R151 1K
R150 33,1W
C122 1/50V
C119 1/50V
C127 .1/50V
C117 .1/50V
C149 27PF/200V
CR12 1N4148
RP9 3.3K
DAC DATA BUS SHT1 A7
ICS SHT1 D5
BR/W SHT1,B7 C5 A6 SHT5,B8
PCIN SHT5,A5
J403
9 KEYING PIN
8 GND
10
2 PIN 1 DRIVER, BANK A
J407
2 PIN 1 DRIVER,BANK B
KEYING PIN
GND
J411
GND
KEYING PIN
J402
24 PIN 1 REMOTE SENSE A
J406
24 PIN 1 REMOTE SENSE B
R13 20K, 1%
R16 4.99K, 1%
U41 LM339
IDBG SHT3 A3
OVRDEN SHT 3 D6
+30V
-15V
-5V
+12V
C59 1/50V
C57 1/50V
C58 1/50V
C56 1/50V
C16-20, 21,24,28,30, 31,32,43,51, 65,70,131 121,123 .1/50V
C62,108,113 116,120 1/50V
J402 20 -5V
J406 20 -5V
21 +12V
9 22 +5V
APPROVALS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED .xx ±.03 .xxx ±.010 ANGULAR
DESIGN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
DRAWN BY SUENEE M
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM D-A DRIVER
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1673
SCALE NONE
SHEET 4 OF 7


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE NHL
NEGATIVE REFERENCE VOLTAGE -5.40V SHT7 D5
U66 AD7524
U72 AD7524
U67 LM318
U68 LM318
U73 LM318
U74 LM318
U71 1436
U69 AD518JH
U70 1436
U75 1436
U41 4011
U45 7406
Q29 MJE 240 HEAT SINK
Q25 2N2907A
Q26 Q27 Q28 2N3725
Q23 Q24 D44H11 D45H11 COMMON HEAT SINK
Q30 Q31 D44H11 D45H11 HEATSINK
Q33 2N2907A
Q35 2N3725
Q36 2N2222
Q52 2N2907A
Q2 MJE240
OVERCURRENT SENSE INTEGRATOR SHT7 D5
J403 PIN 20 DRIVER BANK A
PIN 20 DRIVER BANK B
J407
J402 PIN 20 REMOTE SENSE A
PIN 20 REMOTE SENSE B
J406
J403 PIN 22 DRIVER, BANK A
PIN 22 DRIVER BANK B
J407
J406 PIN 22 REMOTE SENSE B
PIN 22 REMOTE SENSE A
J402
J402 26
J406 26
PRE-CHARGER
DAC DATA BUS SHT1 A7
20 CS SHT1 D5
22 CS SHT1 D5
BR/W SHT4 B8 SHT6,8B
P22EN SHT 1B3
PCCLMP SHT 2 D8
PCIN SHT 4 B8 SHT 6 B8
DB3 SHT 1A3
OVRDEN SHT 3D8
DATA I/O
SCHEMATIC DIAGRAM
D-A DRIVER
DRAWING NO 30-701-1673
SHEET 5OF7


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE
NEG VOLTAGE REF SHT7 C 6 -8.40
POS VOLTAGE REF SHT7 C 6 +8.40
DAC DATA BUS SHT1 A 4
21CS SHT1 D 5
23CS SHT1 D 5
BR/W SHT5,A8 SHT7,A8,D8
P23EN SHT 1 B3
OVERCURRENT SENSE SHT7 D 5
HEATSINK
J403 PIN 21 DRIVER BANK A
J407 PIN 21 DRIVER BANK B
J402 PIN 21 REMOTE SENSE A
J406 PIN 21 REMOTE SENSE B
J403 PIN 23 DRIVER BANK A
J407 PIN 23 DRIVER BANK B
J402 PIN 23 REMOTE SENSE B
J406 PIN 23 REMOTE SENSE A
OMIT
PCIN SHT5 A5
IDB2 SHT 1 A3
OVRDEN SHT 3 D6
IDB4 SHT 1 A3
OVRDEN SHT 3 D6
U62 AD7524
U63 741
U64 741
U65 1436
U76 AD7524
U77 741
U78 1436
U79 1436
U40
U41
Q19 2N2907A
Q20 2N3725
Q21 2N2905A
Q22 2N3725
Q37 MJE 240
Q38 D44H11
Q39 D45H11
Q40 2N2907A
Q41
Q42
Q43 2N2725
Q44 2N2222
CR8 1N4754A (39V)
CR9 1N5392
CR10 1N4148
CR11 1N4148
CR13 1N4148
U45 7406
U46 LM317T
R67 331W
R68 10K
R69 1K
R70 39
R71 10K
R72 33.1W
R73 1K
R74 470
R75 20K
R76 499K,1%
R77 6.65K,1%
R78 5K (10T)
R79 18.2K 1%
R80 10K
R85 18.2K,1%
R86 1K,1%
R112 1K
R130 33.1A
R131 10K
R132 1K
R133 39
R134 33.1W
R135 1K
R136 20K
R137 100
R138 4.75K,1%
R139 24.9K,1%
R140 3.3K
R142 3.3K
R143 24.9K,1%
R144 10K
R145 10K
R178 100K
R12 20K 1%
R18 6.65K 1%
R21 20K 1%
R26 4.99K 1%
C60,C64 1/50V
C66 1/50V
C69 .1/50V
C83 1/50V
C103 .1/50V
C110 1/50V
C112 .1/50V
C114 1/50V
C115 1/50V
C144 .0022/50V
C148 27PF/200V
APPROVALS
DSN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
DRAWN BY R BENN
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM
D-A DRIVER
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1673
SCALE NONE
SHEET 6 OF 7


DIGITAL DATA
SHT 3, A8
U52
74LS02
U55
74LS10
U11
74LS14
U10
74LS74
U60
148
U57
HA1508-5
U59
AD7524
U58
148
U40
339
U6
7406
J409
RAW +10
GND.
J403
PIN 26 DRIVER BANK A
J407
PIN 26 DRIVER BANK B
J402
PIN 26 REMOTE SENSE A
J406
PIN 26 REMOTE SENSE B
J403
PIN 28 DRIVER BANK A
J407
PIN 28 DRIVER BANK B
J402
PIN 28 REMOTE SENSE A
J406
PIN 28 REMOTE SENSE B
Q13 IRF523
Q12 IRF523
Q14 IRF523
Q15 IRF523
COMMON HEAT SINK
FROM OVERCURRENT SENSE INTEGRATOR INPUTS
POS VOLTAGE REF 6.40 SHT6 C8
NEG VOLTAGE REF -6.40 SHT6 D8 SHT5 D8
DAC DATA BUS SHT1 A4
TP4
TP5
TP6
TP7
TP8
+15V
-15V
+5V
-5V
+24.9V
10V ± .010 SHT 5 D6
OVRDEN SHT 3 D6
IDB5 SHT 1A3
IDB6 SHT1 A3
BR/W SHT 6 B8
2628CS SHT1 D5
P26ADD SHT 2C8
P26 CLMP SHT 2D6
OCRST
BBRESET SHT 1,C4
BBCAS SHT 1 C7
BR/W SHT 1,C5
DCHEM SH. 1 B4 SH. 1 C8
15VEN SH1,B3
R165 2.4 2W
R29 430,1W
R36 .33/1W
R34 10K
R33 10K
R32 4.7K
R31 4.7K
R102 4.7K
R60 4.75K,.1%
R59 4.75K,.1%
R57 4.75K,.1%
R58 4.75K,.1%
R37 2.67K,.1%
R171 20K
R36 3.3K
R163 3.3K
R30 1K
R48 1K
R39 1K
R44 4.99K,.1%
R43 100
R42 1K 1/2W
R53 4.99K .1%
R22 10K,1%
R25 10K,1%
R50 1K
R51 1K
R52 4.99K,1%
R46 100
R47 4.99K, 1%
R45 1K 1/2W
R38 4.99K,.1%
R55 11K,.1%
R56 2K 18T
R54 10K,.1%
R23 10K 1%
R24 10K 1%
C41 22/50V
C136 .1/50V
C137 1/50V
C138 .0047 /50V
C139 .001/50V
C48 1/50V
C44 1/50V
C140 .001/50V
C42 0047 50V
Q8 2N3725
Q7 2N2907A
Q6 2N2907A
Q9 MJE361
Q8 2N2222
Q10 2N2222
CR1 1N4731A 4.3V
CR7 1N4148
CR20 IN4148
CR19 1N5817
REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
E SEE SHEET ONE NHL
APPROVALS
DSN ENGR
MFG ENGR
QUAL ASSUR
ENGR MGR
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
ANGULAR
DRAWN BY R BENN
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM
D-A DRIVER
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1673
SCALE NONE

Warranty One Year

Data I/O warrants that all equipment sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for one year. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect; if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to Data I/O's facility shall be borne on account of buyer, including all duties, fees, brokerage and special handling charges. Shipment from Data I/O's facility shall be borne by Data I/O.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCHANTABILITY AND THE WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE. 0299/1284

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Reader Comments
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P.O. Box 97046
Redmond, WA 98073-9987

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual? _____

How can this manual be improved? _____

_____

_____

Additional comments: _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____ Manual or Part No. _____

Warranty/Registration

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? ☐ YES ☐ NO

Did this equipment arrive intact, without loose parts or cable damage? ☐ YES ☐ NO

Did the equipment operate on power-up? ☐ YES ☐ NO

Did you attain adequate system performance? ☐ YES ☐ NO

Were any electrical adjustments required? ☐ YES ☐ NO

If you required assistance, was a local Data I/O representative contacted? ☐ YES ☐ NO

Comments: _____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

U.S. Sales Offices and Representatives
Direct Sales and Service Offices

Data I/O Corporation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
Telex Dom. 15-2167,
Int'l. 4740166 DIO UI

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Data I/O Corporation
1700 Wyatt Drive
Suite 1
Santa Clara, CA 95054
(408) 727-0641

SOUTHWEST REGION

Data I/O Corporation
2770 South Harbor Blvd.
Suite K
Santa Ana, CA 92704
(714) 662-1182 *(Sales)*
(714) 662-2498 *(Service)*
Telex 755870

EASTERN REGION

Data I/O Corporation
Nashua Road
Route 101A
Amherst, NH 03031
(603) 889-8511 *(Sales)*
(603) 889-8513 *(Service)*
Telex 943431

CENTRAL REGION

Data I/O Corporation
1810 N. Glenville Drive
Suite 108
Richardson, TX 75081
(214) 235-0044
Telex 792474

Representatives

ALASKA, WASHINGTON (TRI-CITIES, VANCOUVER), OREGON

Northwest Test and Measurement
8196 Southwest Hall
Suite 217
Beaverton, OR 97005
(503) 646-9966
1-800-247-5700
Telex 910-467-8775

WESTERN WASHINGTON, SPOKANE

Northwest Test and Measurement
4020 148th Ave. N.E.
Suite F
Redmond, WA 98052
(206) 881-8857

ARKANSAS, LOUISIANA, OKLAHOMA, TEXAS

TESTECH, Inc.
1000 E. Campbell Road
Suite 108
Richardson, TX 75081
(214) 644-5010

4800 West 34th St.
Suite D-6
Houston, TX 77092
(713) 956-0837

1715 Capital of Texas Hwy S.
Suite 107
Austin, TX 78746
(512) 327-7033

OHIO

Electro Sales Associates
1635 Mardon Drive
Dayton, OH 45432
(513) 426-5551

26250 Euclid Avenue
Suite 331
Cleveland, OH 44132
(216) 261-5440

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Livonia, MI 48152
(313) 474-7320

9816 Portage Road
Portage, MI 49002
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Electro Sales Associates
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Allison Park, PA 15101
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UPSTATE NEW YORK

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Building D
Fayetteville, NY 13066
(315) 446-0220

KANSAS, NEBRASKA

Midtec Associates, Inc.
7702 Mize Road
DeSoto, KS 66018
(913) 441-6565
Telex 910-743-4129

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Midtec Associates, Inc.
8460 Lindbergh North
Suite 11
Florissant, MO 63031
(314) 837-5200

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Deerfield Beach, FL 33441
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1398 Semoran Blvd.
Suite 106
Casselberry, FL 32707
(305) 645-3444

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Pen Tech Associates
627 Cherokee Street
Suite 21
Marietta, GA 30060
(404) 424-1931

NORTHERN FLORIDA, ALABAMA, TENNESSEE, MISSISSIPPI

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3322 Memorial Pkwy. S.W.
Suite 36
Huntsville, AL 35801
(205) 881-9298

NORTH CAROLINA, SOUTH CAROLINA

Pen Tech Associates
3709 Alliance Drive
Suite C
Greensboro, NC 27407
(919) 852-6000

MINNESOTA, NORTH DAKOTA, SOUTH DAKOTA

Torkelson Associates
4940 Viking Drive
Minneapolis, MN 55435
(612) 835-2414
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